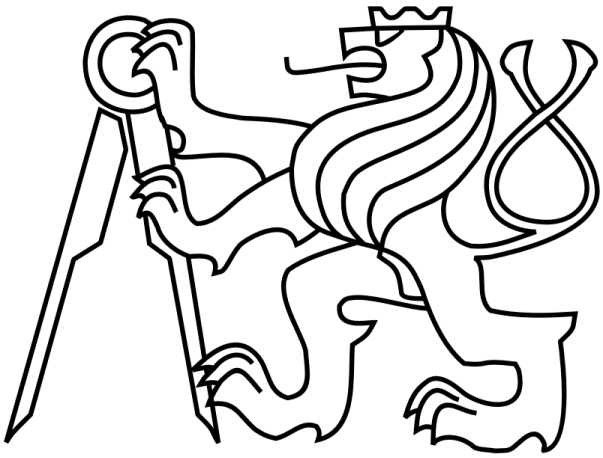
CZECH TECHNICAL UNIVERSITY IN PRAGUE

FACULTY OF ELECTRICAL ENGINEERING



DIPLOMA THESIS

2014 **Bc. Martin Jelínek**

České vysoké učení technické v Praze
Fakulta elektrotechnická

katedra mikroelektroniky

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: **Bc. J E L Í N E K Martin**

Studijní program: Komunikace, multimédia a elektronika
Obor: Elektronika

Název tématu: **Návrh spínaného zdroje typu Buck pro 4-jádrový ARM procesor**

Pokyny pro vypracování:

1. Prostudujte dostupnou literaturu týkající se možností řízení spínaných zdrojů.
2. Na základě 1) navrhněte modely spínaných zdrojů v prostředí MATLAB/Simulink a zvažte jejich možnosti vícefázového paralelního řazení.
3. Diskutujte metody pro rovnoměrné proudové zatížení multifázového zdroje a aplikujte je na vzniklé modely zdrojů.
4. Z uvažovaných metod vyberte tu nejvhodnější metodu jak napájet 4-jádrový ARM procesor se špičkovým ztrátovým výkonem 12 W (10 A @ 1.2 V). Odůvodněte svoji volbu.
5. Zhodnoťte možnosti integrace vybrané architektury pro mobilní aplikace.

Seznam odborné literatury:

[1] Suman, G.; Kumar, B.V.S.P.; Kumar, M.S.; Babu, B.C.; Subhashini, K.R., "Modeling, Analysis and Design of Synchronous Buck Converter Using State Space Averaging Technique for PV Energy System," Electronic System Design (ISED), 2012 International Symposium on , vol., no., pp.281,285, 19-22 Dec. 2012
[2] Chieh-Chuan Feng, "A robust composite control for basic DC-DC converters," Control Conference (CCC), 2012 31st Chinese , vol., no., pp.4769,4774, 25-27 July 2012
[3] Chang-Shiarn Lin; Chen, Chern-Lin, "Single-wire current-share paralleling of current-mode-controlled DC power supplies," Industrial Electronics, IEEE Transactions on, vol.47, no.4, pp.780,786, Aug 2000
[4] Abu-Qahouq, J.A.; Huang, L.; Huard, D., "Sensorless Current Sharing Analysis and Scheme For Multiphase Converters," Power Electronics, IEEE Transactions on , vol.23, no.5, pp.2237,2247, Sept. 2008

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Platnost zadání: 31. 8. 2015

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V Praze dne 12. 2. 2014

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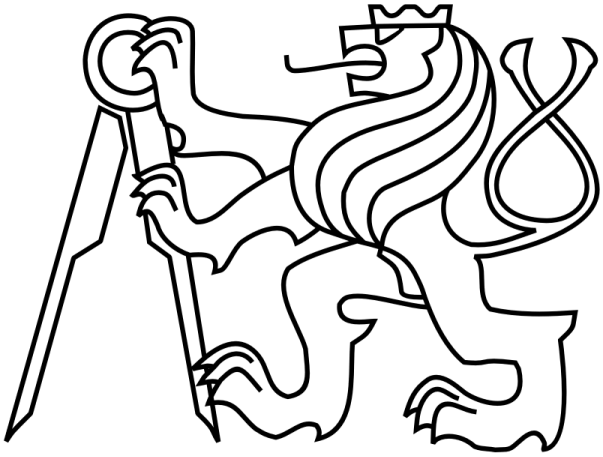


Diploma thesis

Design of a Buck type SMPS for 4-core ARM processor

Author: Bc. Jelínek Martin

Supervisor: Ing. Jiří Jakovenko, Ph.D

Prague, 2014

Declaration

I declare I have completed my diploma thesis on my own with the contribution of my supervisor and consultants. I used only materials (literature, projects, articles) specified in the list of references. I agree with the utilisation of the information presented in my thesis pursuant to Copyright Act 121/2000 Coll., Sec. 60.

Prohlašuji, že jsem zadanou diplomovou práci „**Návrh spínaného zdroje typu Buck pro 4-jádrový ARM procesor**“ zpracoval sám s přispěním vedoucího práce a používal jsem pouze literaturu uvedenou na konci práce. Souhlasím se zapůjčováním práce a jejím zveřejňováním.

Prague ....

signature

Acknowledgements

I would like to thank team from ST Microelectronics and to the company as such, for their patience, time and valuable expertise they have provided me during my work. It would not be possible to work on this challenging topic without their great support. Also, I would like to thank my supervisor Ing. Jiří Jakovenko, Ph.D. for appreciate advises. His comments and suggestions helped me to improve my work. Finally I would like to thank my family and friends for their disinterested support during the time of my studies.

Abstract

This Diploma thesis deals with a design of Buck type multiphase switched-mode power supply. Also it describes how to model this type of SMPS and possibilities how to parallelize Bucks depending on the control mode and operating conditions. The environment of Matlab/Simulink is used for the analysis and simulations. The creation of the Buck's power stage model is described. The most frequently approaches to the problem solving were chosen: voltage mode, current mode and hysteretic mode control. These control modes and their variations are described. Their multi-phasing and current balancing possibilities are discussed. A new control method for the hysteretic controlled multiphase Buck is proposed. Common values with their supposed tolerances typical for mobile devices are used in simulations.

Anotace

Tato diplomová práce se zabývá problematikou návrhu vícefázového snižujícího spínaného zdroje typu Buck. Zároveň se zabývá problematikou modelování spínaného zdroje a jeho možnostech paralelního řazení v závislosti na pracovním módu a na pracovních podmínkách zdroje. Jako vývojové prostředí pro analýzu a simulace je zvolen Matlab/Simulink. Je zde popsán modelu výkonové části spínaného zdroje. Jako nejčastěji užívané metody pro řízení byly zvoleny: napěťový mód, proudový a hysterezní mód řízení. Tyto možnosti řízení s možnými variacemi jsou popsány. Je navržen nový způsob řízení vícefázového spínaného zdroje pracující v hysterezním módu. Možnosti sloučení a proudového vyvážení více fází jsou porovnány. Pro srovnání a simulace jsou použity hodnoty součástek, které jsou typické pro malá přenosná zařízení.

Contents

Nomenclature

η	%	efficiency
μ_r	-	relative permeability
ϕ	°	phase shift
ω	s^{-1}	angular frequency
ω_p	s^{-1}	angular frequency of pole
ω_s	s^{-1}	switching frequency
ω_{ESR}	s^{-1}	angular frequency of zero caused by capacitor ESR
C	F	capacitor value
C_{out}	F	output capacitor value
C_g	F	gate capacity
ESR	Ω	effective series resistance
D	-	duty cycle
D_{max}	-	maximal duty cycle
f	Hz	frequency
f_s	Hz	operating frequency
f_C	Hz	crossover frequency
G_m	-	gain margin
I_{out}	A	output/load current
I_L	A	inductor current
I_{ratio}	-	current imbalance between phases
L	H	inductor value
L_{Av}	H	average inductor value
N	-	phase number
N_{max}	-	maximal number of phases
P_i	W	inductor loss
P_{hys}	W	hysteresis loss
P_{ec}	W	eddy current loss
P_r	W	residual loss

P_m	°	phase margin
PWM_{gain}	-	gain of PWM modulator
p	%	voltage/current ripple
p_{imb}	%	current imbalance in multiphase power supply
p_{hyst}	%	p_{imb} in hysteretic mode controlled multiphase power supply
Q	-	quality of resonant circuit
R_{load}	Ω	load resistance
R_{dsON}	Ω	drain-source on resistance
R_{dsOFF}	Ω	drain-source off resistance
R_{onH}	Ω	high-side MOS on resistance
R_{onL}	Ω	low-side MOS on resistance
R_{sw}	Ω	switch on resistance
R_L	Ω	coil resistance
R_C	Ω	capacitor resistance/ESR
R_{sen}	Ω	transresistance of current sensor
S	-	technology scaling factor
T_s	s	switching period
T_{pulse}	s	pulse generation period
T_{ON}	s	pulse duration
t_{ON}	s	on-time
V_{in}	V	supply voltage
V_{out}	V	output voltage
V_e	V	error voltage
V_{ref}	V	reference voltage
V_{ramp}	V	ramp generator voltage
V_{bal}	V	current balance voltage
V_c	V	control voltage
V_i	V	voltage representation of inductor current
V_{win}	V	hysteresis window
V_{com}	V	comparator's output voltage

CCM	continuous conduction mode
CM	current mode
COT	constant on-time controller
CPU	central processing unit
DC	mean value of the waveform
DCM	discontinuous conduction mode
EMI	electromagnetic interference
HMOS	high-side metal oxide semiconductor field effect transistor
LC	inductor-capacitor circuit
LMOS	low-side metal oxide semiconductor field effect transistor
MOSFET	metal oxide semiconductor field effect transistor
PWM	pulse width modulation
RC	resistor-capacitor circuit
RF	radio frequency
SMPS	switched-mode power supply
SR	set reset latch
VM	voltage mode

1. Introduction

Nowadays, we observe still evolving world of electronics, especially small portable devices. Should the new device take hold in the market, it is necessary to meet the ever greater demands that are often contradictory. The result is a compromise solution within a given technology. The customer wants a new feature, which means higher computing power, and at the same time he wants to protect the environment. The same applies to the requirement of small and light portable equipment and long battery life. The solution is low voltage and low power technology. This places challenging demands on the work of designers who have to meet increasingly stringent specifications. Principal parameter for a new production technology is the scaling factor *S*, the typical value is $\sqrt{2}$. This means that the demands of today's processors to power supplies continues to grow, especially demand for its output voltage even at large and fast load transients.

Power supply voltage of CPUs decreases with each new technology proportionally with $1/S$. Power dissipation does not decrease, this makes it difficult to design an SMPS (switched-mode power supply), which must be able to supply relatively large currents. The above affects the efficiency of resources, represents an increase of influence of parasitic resistances and this has resulted in an increase of conductivity losses. Other pitfalls of the proposal are physical properties of ferromagnets, which limit the maximum switching frequency, the maximum currents and weight, which is undesirable in mobile devices. This limitation can be overcome by using a multi-phase source. At the same time we are able to improve other parameters of the source due to right timing.

Proper phasing and managing several phases is a very challenging task. It is important to know whether the behavior of the respective single-phase source is suitable for parallelize, or how to modify it and force it to cooperate.

1.1 Basic parameters of sources

Power supply is an element that regulates voltage and current relationships in the circuit. Parameters of the sources describe these relationships. There are many ways to divide them. Here is one way:

- numerical parameters
- electrical characteristics

Another option is separation into static and dynamic parameters. Numerical parameters are:

- supply voltage range - V_{in}
- nominal output voltage - V_{out}
- maximum load current - I_{out}
- maximum output voltage ripple - p
- operating frequency - f_s
- efficiency - η
- percentage of current imbalance in multiphase power supply - p_{imb}
- others

Sometimes it is necessary to define the parameters in dependence on working conditions. These characteristics are typically given in tables or in charts:

- load output characteristic - $V_{out} = f(I_{out})$
- load transient - $V_{out} = f(\Delta I_{out})$
- line transient - $V_{out} = f(\Delta V_{in})$

The aforementioned parameters depend on the characteristics of power stage, LC filter and the feedback loop. The voltage overshoot or undershoot of the output voltage during fast load changes, its size and duration is determined by the change of ΔI_{out} and bandwidth of the closed loop. We will compare the different designs mainly according to these parameters.

1.2 Processor requirements (4-core ARM)

In this work, the processor type is not specified, we haven't exactly specified requirements. However, we assume that a CPU is powered from one lithium-ion battery which nominal value is 3.7 V. This defines the range of input voltage **[15]**, the range is from discharge cut-off voltage 2.75 V to charge cut-off voltage 4.2 V. The processor supply voltage is around 1 V, which is usually adjustable according to the operating mode. So low supply voltage is used to reduce gate charge capacity losses.

Processor's maximum power consumption is 12 W and if we are limited by the current about 3 A, see chapter 2.2, we must use a multiphase SMPS with 3-4 phases. The CPU consumption isn't stable, but can change very quickly. The power supply must meet the voltage tolerance even at sudden changes of consumption, a load transient could have rising and falling edge faster than the working period of SMPS. Processors operate at frequencies in the GHz units, but SMPSs operate only at several MHz units. The output voltage may vary within a tolerance of ± 3% **[16]**. The above limits are very difficult to achieve especially for processors with high power consumption. Therefore, some processors are designed so that they can change the power consumption only after certain jumps, never the full range. It can be designed directly or via software. Voltage deviation under load transient as an SMPS parameter is usually defined with change between 10% and 90% of maximal load with rising/falling edge time of 100ns.

Accuracy of SMPS operating frequency is critical in some applications, especially in RF applications, but in this proposal is not required.

2. Basic principle and architecture of step down power supply

To decrease DC voltage we have two basic possibilities:

- use linear regulator
- use SMPS i.e. switched-mode power supply

A linear regulator has low efficiency in operations when ratio V_{in}/V_{out} is high. It operates as a variable resistance which dissipates excess power as heat. SMPS, on the other hand, uses storage element. Charge pumps use capacitors, Bucks converters use inductors. At first sight it may be said, that the quality of these storage elements determines efficiency of conversion.

2.1 Principle of step down SMPS-Buck

An elementary block of the proposed source is switched source called Buck. The simplified diagram is shown in figure 2.1 **[4]**.

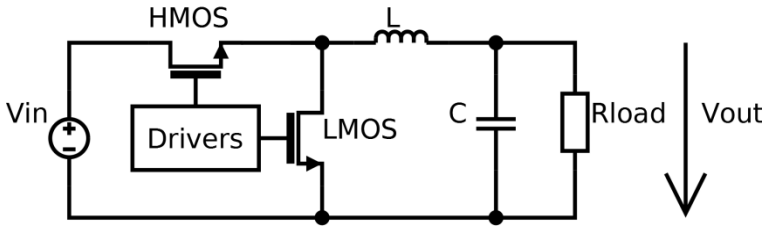


Figure 2.1: Block diagram of a Buck SMPS

Initially HMOS is on and LMOS is off, current flows from the source V_{in} through the HMOS and the inductor L to the load R_{load} and to the output filter capacitor C. Then HMOS is off and LMOS is on, current flows from the inductor L to the load and to the output filter capacitor via the switch LMOS. The inductor L is the source. A simplified version consists of a diode replaced as switch HMOS, this version is called synchronous buck. Neglecting losses equation (1) **[6]** applies to the output voltage V_{out}.

$$V_{out(ideal)} = \frac{t_{on}}{T_s}.V_{in} = D.V_{in}\ [V], \qquad (1)$$

where t_{on} is the duration of switched HMOS, T_s is the switching period, D is the duty cycle of switching HMOS.

2.2 Limitation of single-phase SMPS

If we need to supply high power load, the first idea would be to oversize the single-phase source. This solution is possible, but will result in many problems. Imagine that we need to double the desired output current I_{out} while maintaining the other properties of the source.

First, you will need to customize a coil for the desired output current, i.e. customize for core saturation. It's possible to saturate the core because there is a limit to the level of magnetic flux in a real inductor. When this occurs the relative permeability μ_r falls and this causes the level of inductance value to be the same as the coreless coil as can be seen in figure 2.2. To avoid this, we double the coil core volume.

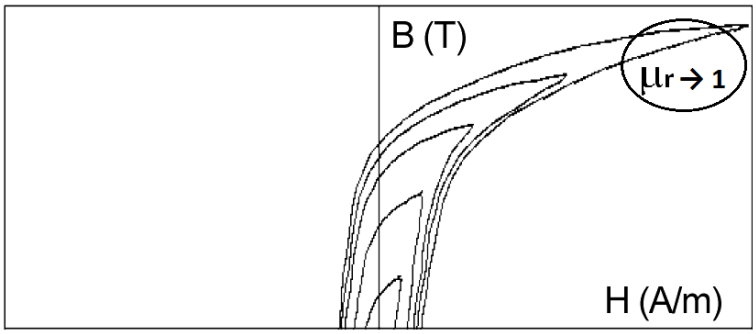


Figure 2.2.: One half of B-H hysteresis loop **[17]**

For the output capacitor C_{out} and its effective series resistance ESR_C equations (2) **[1]** are valid.

$$C_{out} > \frac{I_{out} \cdot D \cdot T_s}{\Delta V_{out}}, \tag{2a}$$

$$ESR_C < \frac{\Delta V_{out}}{\frac{I_{out}}{1-D} + \frac{\Delta I_L}{2}}, \tag{2b}$$

$$\Delta I_L = \frac{(V_{in} - V_{out}) \cdot D \cdot T_s}{L}, \tag{2c}$$

where ΔV_{out} is output voltage ripple, ΔI_L inductor current ripple, that stays the same. This method represents a doubling of all key elements, including switches that have to switch double currents.

The proposal can be modified by doubling the operating frequency; then half the inductance L is sufficient for the same ΔI_L and the volume of the core is kept same, for the reasons already said. The capacitor will need to have better ESR only. Any increase in frequency results in an increase of losses:

- switching losses
- inductor core losses

As switching elements we usually use MOSFET transistors. At each switch on and switch off, you must charge or discharge gate capacity C_g, it represents a loss increasing linearly with frequency. Next frequency dependent losses are losses in the transition between R_{dsON} and R_{dsOFF} of the switch, assuming constant closing and opening time with increasing frequency. These losses are called switching losses.

Another problem is the losses in ferrites in inductors P_i **[18]**. These are also frequency dependent.

$$P_i = P_{hys} + P_{ec} + P_r, \quad (3)$$

where P_{hys} is hysteresis loss, P_{ec} is eddy current loss, P_r is residual loss.

It is known that the hysteresis loss rises linearly with increasing frequency. The eddy current loss rises with square of frequency. Fortunately it is found that the hysteresis loss is the dominant core loss up to a frequency determined by the performance of the core. It is clear that increasing the frequency is not a simple recipe for success. Compared to the first solution, we save on the volume of the capacitor, the price is lower, but the efficiency is reduced due to higher losses.

Let's take the positive aspects of both approaches. Reduce the output capacitor, but keep the same parameters such as efficiency, operating frequency and etc. The solution is a multi-phase SMPS.

2.3 Principles and advantages of multiphase SMPS

In order to increase performance we need multi-phase SMPS. The concept of multi-phase buck SMPS is shown in figure 2.31 **[4]**, where you see the way of adding phase.

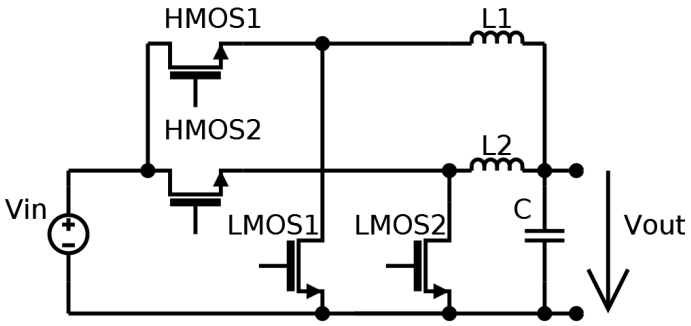


Figure 2.31: Block diagram of a two-phase SMPS buck

Typically, the phases are uniformly switched in time, this technique is called interleaving. If the phases are well phased and currents in each phase are known, there is a ripple cancellation effect. The ripple current on both input and output sides is significantly reduced, resulting in reduction of input and output capacitors. Also lower inductance values can be used, and transient response can be subsequently improved. The ripple cancellation effect is simply a result

of Kirchoff's current law. Each phase currents are added together in a single input /output current. The value of ripple p can be calculated by equation (4), where $i_{out(p-p)}$ is the current peak-to-peak and i_{out} is the average current.

$$p = \frac{i_{out(p-p)} \cdot 100}{i_{out}} \ [\%] \qquad (4)$$

Figure 2.32 shows the waveform of the output current ripple *p* depending on the duty cycle *D* for the phases which are evenly shifted, every phase of SMPS works on the threshold of a continuous mode.

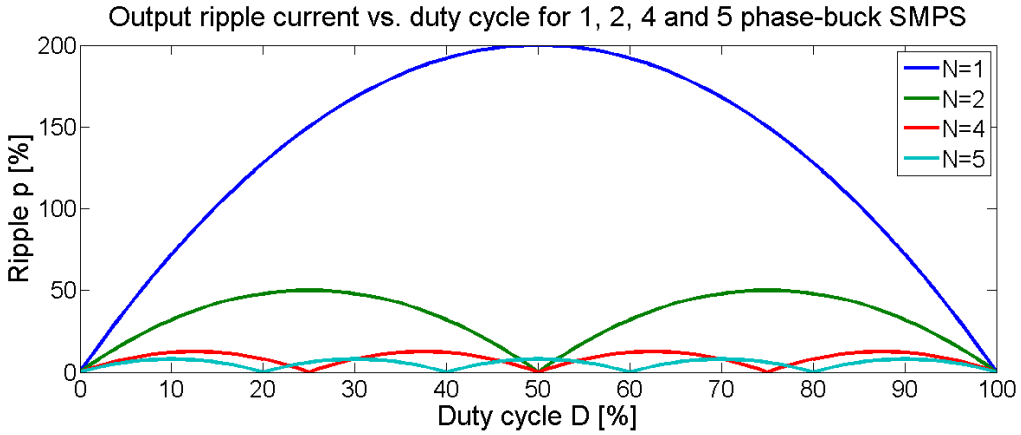


Figure 2.32: An example of ripple cancellation effect **[19]**

The disadvantage of a powerful source is inefficiency at light loads. But in multi-phase SMPS we could use phase shedding, which improves efficiency in multiphase converter by dynamically changing the number of phases, figure 2.33 is inspired in **[20]**.

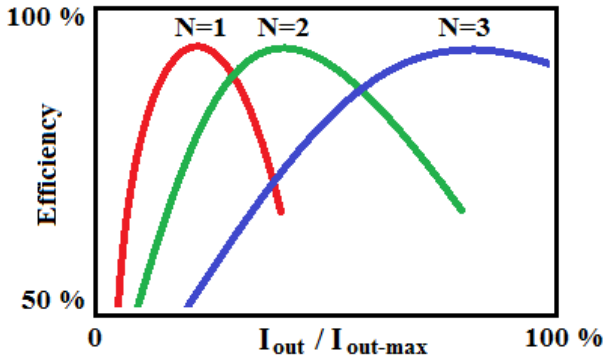


Figure 2.33: Efficiency in dependence on number of phases

At light loads it uses only a few phases and when loads rise it adds one more phase. It complicates whole design, because there is a demand for current sensing. This is not the biggest

problem because multi-phase SMPS needs to know the current in each branch for current balancing. Good current sharing ensures even thermal distribution and high reliability of the system. Current mode controlled bucks are usually preferred, because of their inherent ability to current sharing in steady state and during transients. But they have complicated design, thanks to more control loops.

2.4 Current imbalance in multiphase SMPS buck

Current balance would be theoretically necessary if we had exactly the same phases. Imbalance depends on:

- ratio of the value of components
- heat distribution
- aging

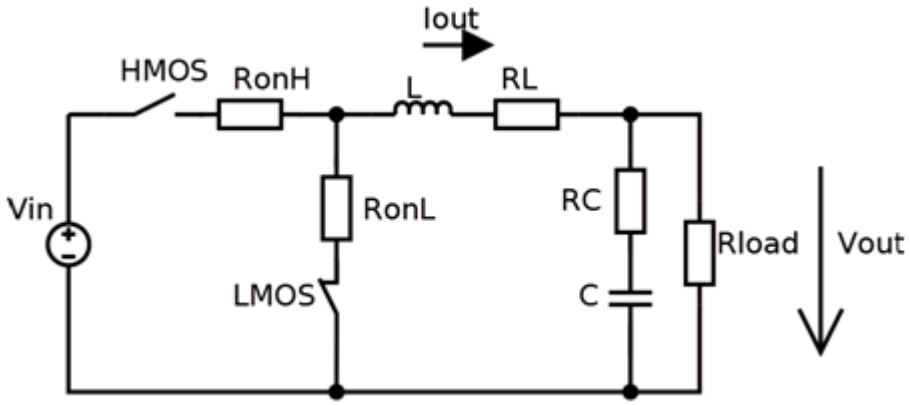


Figure 2.41: Block diagram of a simplified model of buck

Figure 2.41 shows the practical equivalent buck model. This scheme differs from the block diagram in included parasitic resistance. The resistance of the switches R_{onH} and R_{onL} and the sum of serial resistance of the coil and resistance of layout R_L have the greatest impact on imbalance. Then we can define the relationship of duty cycle *D* [**4**].

$$D = \frac{V_{out}+I_{out}(R_{onL}+R_L)}{V_{in}+I_{out}(R_{onL}-R_{onH})}, \quad (5)$$

where I_{out} is current in one phase. For example for two-phase buck without some current balancing mechanism the duty cycle must be the same for both phases, then:

$$I_{ratio} = \frac{I_{out1}}{I_{out2}} = \frac{R_{onL}+R_{L2}-D(R_{onL}+R_{onH})}{R_{onL}+R_{L1}-D(R_{onL}+R_{onH})} = \frac{R_{sw}+R_{L2}}{R_{sw}+R_{L1}}, \quad (6)$$

where I_{ratio} is current imbalance between two phases, indexes indicate phases, R_{sw} represents R_{on} of switches, we assume that they have identical values or just ratios, because they are integrated on one chip.

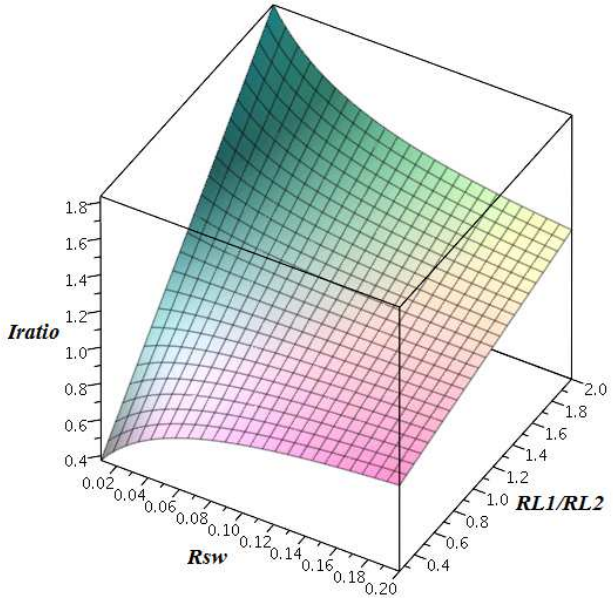


Figure 2.42: Chart of equation (6), $R_{sw} = 10 \,..\, 200\text{m}\Omega$, $R_{L1} = 50\text{m}\Omega$

In Figure 2.42 we can see the dependence of current imbalance depending on the relative values of R_L and depending on R_{sw}. There is a solution for high voltage and low current applications, high resistance R_{sw} helps reduce the impact of tolerances R_L. In our case, this suppression is not possible due to large losses. We need some active solutions, not just suppress the influence of asymmetry.

Other aspects are different flip times of driver circuits and different coils which inductance can make mistaken current measurements. This depends on the operating mode of SMPS, it's explained later in chapter **Control mode**.

Table of components tolerances:

Part	Tolerance	Common value
R_{dsON}	20%	100mΩ
R_L	50%*	50mΩ
L	20%	2μH

*depends on proper design layout

3. Mathematical apparatus

For a description of the issue, I prefer the superstructure of MATLAB - Simulink because it allows to easily and quickly implement models of dynamic systems in the form of block diagrams. Main features are:

- determines the behavior of dynamic system - time solution (simulation)
- enables the design of control systems, arbitrary control loop
- contains libraries of input signals to determine the control response
- wide range of libraries - Toolboxes
- easy modelling and simulation of various solutions

One disadvantage is the need to know the mathematical description of the problem, which may not always be trivial. For this reason it is necessary to compare the simulation results with theoretical knowledge, because the results may be based on the wrong model. Circuit simulator gives greater certainty, it is better linked to the realization of the real components, but this is usually compensated by more time-consuming simulations.

3.1 Implementation of circuits in MATLAB/Simulink

A switching power supply changes its operation mode as a function of the switch ON or OFF state. It is a discrete and nonlinear system, as we can see in figure 3.1. To analyze the feedback loop with the linear control method, a linear small signal model is needed.

First, we reduce the complexity of the circuit by replacing the real components with their simplified models of the ideal elements, figure 2.41.

Then, if we assume synchronous mode of buck converter for circuit description. We split the circuit into two working phases: ON and OFF. Only the switch HMOS is turned ON in the phase ON, in the phase OFF only the LMOS. Now the problem is simplified to two dynamic systems, for the simulation we use the block State-Space [**2**].

Dynamic equations of state-space representation of a linear system are written in the following form:

$$\dot{\vec{x}}(t) = A.\vec{x}(t) + B.\vec{u}(t), \qquad (7a)$$

$$\vec{y}(t) = C.\vec{x}(t) + D.\vec{u}(t). \quad (7b)$$

$\vec{x}(t)$ is the state vector determining the state of the system, $\dot{\vec{x}}(t) = \frac{d\vec{x}}{dt}$,

$\vec{y}(t)$ is the output vector of the system,

$\vec{u}(t)$ is the input vector of the system,

A, *B*, *C*, *D* are matrices of dynamics of the system, input and output matrices and matrix of direct action input to output.

Because the description of the circuit is divided into two phases, it is necessary to have two sets of equations for description. At the buck's output is a current source, that represents the current consumed from its output. As output we require output voltage v_{out} and coil current i_L.

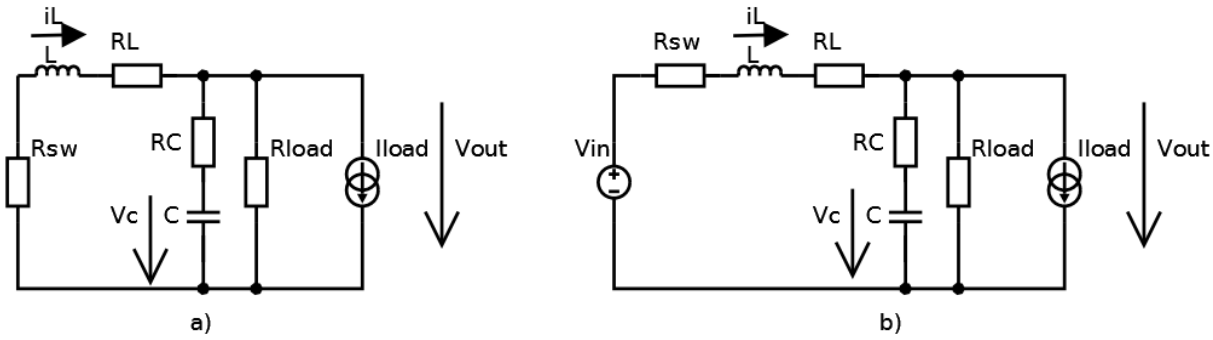


Figure 3.1: Buck's model dividend into: a) phase OFF b) phase ON

$$x = \begin{pmatrix} i_L \\ v_C \end{pmatrix}, y = \begin{pmatrix} i_L \\ v_{out} \end{pmatrix}, u = \begin{pmatrix} i_{Load} \\ v_{in} \end{pmatrix}$$

$$\dot{x}_1 = \begin{pmatrix} \frac{-(R_{sw}R_C + R_{sw}R_{Load} + R_CR_{Load} + R_LR_C + R_LR_{Load})i_L - R_{Load}u_C + R_LR_{Load}i_L}{L(R_C + R_{Load})} \\ \frac{R_{Load}i_L - u_C - R_{Load}i_{Load}}{C(R_C + R_{Load})} \end{pmatrix}$$

$$\dot{x}_2 = \dot{x}_1 + \begin{pmatrix} \frac{v_{in}}{L} \\ 0 \end{pmatrix}$$

$$y_{1,2} = \begin{pmatrix} i_L \\ \frac{R_{Load}R_Ci_L + R_{Load}v_C - R_{Load}R_Ci_{Load}}{R_C + R_{Load}} \end{pmatrix} \quad (8)$$

The equation (8) shows the structure of matrices A, B, C, D, which is necessary to assemble the circuit description in Simulink using the state-space block. The set of equations $\dot{x}_1, y_1$ is for the phase OFF. Note that equations describing the state of the system evidently depend on the working phase circuit.

For a description of N-phase buck it is necessary to assemble always 2^N sets of equations, the state vector x consists of N +1 elements, since it has one output capacitor and the N coils, information about the state of storage elements must be always calculated. For simulations is used the state-space block which allows to dynamically change the state-space matrices, this is the invention of ST Microelectronics.

Now we have solved the power stage representation in simulation environment Simulink in the state-space description. For further work it is necessary to calculate certain transfer functions to determine stability. Transfer functions are obtained by transferring state space representation using function *ss2tf*. For a voltage mode to obtain the Laplace image $TF\_V(s) = \frac{v_{out}}{v_{in}}$, it is possible to draw from equations (8), we obtain state space system (9). In the same way it is possible to get the transfer function $TF\_I(s) = \frac{I_L}{v_{in}}$, that is required to analyze a buck source in the current mode.

$$x_V = \begin{pmatrix} i_L \\ v_C \end{pmatrix}, y_V = v_{out}, u_V = v_{in}$$

$$\dot{x}_V = \begin{pmatrix} \frac{-(R_{sw}R_C + R_{sw}R_{Load} + R_CR_{Load} + R_LR_C + R_LR_{Load})i_L - R_{Load}v_C + R_LR_{Load}i_L}{L(R_C + R_{Load})} + \frac{v_{in}}{L} \\ \frac{R_{Load}i_L - v_C}{C(R_C + R_{Load})} \end{pmatrix}$$

$$y_V = \frac{R_{Load}R_Ci_L + R_{Load}u_C}{R_C + R_{Load}} \qquad (9)$$

Because of the output LC filter, the linear small signal transfer function *TF_V* is actually a second-order system with two poles and one zero, as shown:

$$TF\_V(s) = \frac{\left(\frac{s}{\omega_{ESR}} + 1\right)}{\left(\frac{s}{\omega_p}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_p}\right) + 1}, \qquad (10)$$

where Q is peaking of LC pole. There are double poles ω_p located at the resonant frequency of the output inductor and capacitor. There is a zero ω_{ESR} determined by the output capacitance and the capacitor effective series resistance.

3.2 Stability criterion

Stability is one of the basic requirements that are placed on the closed-loop system **[5]**. Whole system is stable, if the system is biased of the equilibrium and the disappearance of the

external forces that caused this deviation, the controlled system over time will return to its original equilibrium. In other words, the stability of the controlled system is to keep around equilibrium or return to it after remission of external forces. The system is stable when the limited input signal produces a limited output signal in response.

From the viewpoint of stability, the controlled system is divided into stable, on the border of stability and unstable. It is always required that the closed-loop system is stable under all conditions. It is clear that parameters and dynamic characteristics of the controlled system are given by the system design, technology and etc. It is not easy to change it. We can only change the dynamic properties of the regulator by adjusting its optional parameters. Thus stability and other properties of closed-loop system can be achieved.

There are many ways to determining stability. This chapter will not cover all the possible criteria for the establishment of a stable system. I'd just like to explain a minimum basis for further consideration.

Frequency characteristic is a graphical representation of the transfer function $G(j\omega)$, where the angular frequency ω goes from 0 to ∞. Using the frequency characteristics is considered to be the most common way to determine the stability of controlled systems.

The definition of stability under the simplified Nyquist criteria, in logarithmic coordinates is shown in figure 3.2. Closed-loop system is stable, if its open-loop gain crosses 1 (0 dB) only once, the system is stable if the phase $\phi(\omega)$ at the crossover frequency f_C is more than -180°, if not the loop will oscillate at frequency f_C.

On the frequency response for open-loop system, we define quality indicators of regulation phase margin P_m and gain margin G_m, which are defined in figure 3.2.

The phase margin is the amount by which the phase at f_C is higher than the critical value of -180°. The gain margin is the amount of gain increase required to make the loop gain unity or zero in dB at the frequency where the phase shift is -180°.

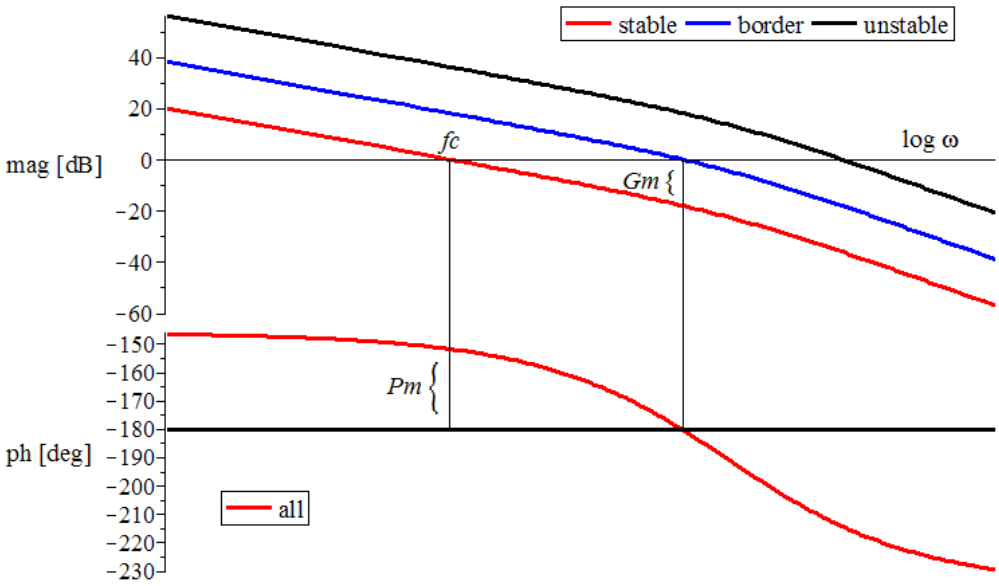


Figure 3.2: An example of open-loop transfer function for demonstrating the simplified Nyquist stability criteria

If the phase margin is only a few degrees, the system tends to be unstable, it exhibits considerable overshoot and ringing at crossover frequency. This is the case with an undercompensated system. Typical symptoms of an undercompensated SMPS are acoustic noise of electric components, irregular switching waveforms, oscillation of output voltage. Vice versa, an overcompensated system can be very stable, but the cost is usually a slow transient response. Then the design requires excessive output capacitance to meet transient specification, increasing the total cost and size. An optimum loop compensation design is stable and quiet, but is not overcompensated, so it has a fast response and the output capacitance should be minimized.

The performance of the closed voltage regulation loop is evaluated by the loop bandwidth and the loop stability margin. The loop bandwidth is defined by the crossover frequency f_C. The loop stability margin is typically quantified by the phase margin or gain margin. For a buck converter, typically 45° phase margin and 10 dB gain margin is considered sufficient [**6**]. This provides good response with a little overshoot, but no ringing. But if the loop gain for a moment decreases so that f_C moves down into the frequency range where the phase margin is less 0°, conditional stability is broken and the loop becomes unstable. It can happen when the system runs into load step and the feedback should go to saturation, for example. Then the system will oscillate and probably never recover.

4. Operating conditions of buck

As already mentioned, the properties of the controlled system are given by topology, so in this chapter we will focus on different concepts. It is clear that they mostly affect the properties and characteristics of SMPS.

4.1 Conduction mode

The design of an SMPS is associated with the term ‘conduction mode’. It can be divided into continuous and discontinuous conduction mode CCM / DCM. It is defined by the properties of the inductor current waveform **[1]**. DCM can be found in non-synchronous SMPSs when inductor ripple current is more than average output current. The inductor current stays at zero during part of the period. At that moment oscillation and higher interference due to discontinuities may occur.

It would seem, that DCM is not possible in the synchronous buck converter. In CCM at light loads the inductor current crosses zero. If we are able to detect this crossing, then the lower switch LMOS can be turned off. This helps to reduce conduction losses and increase efficiency. But in the following description, this possibility will not be discussed.

4.2 Control mode

The kind of control mode determines how the exact value of the output voltage and how its stability is achieved. The basic control methods are:

- voltage mode control
- current mode control
- hysteretic mode control
- no control

The last option on the list will not be further discussed. It should only be used in applications where the load is constant or precise output voltage is not required.

4.2.1 Voltage mode control

The output voltage is regulated by a system shown in figure 4.2.11. This scheme is referred to as voltage mode control. There is only one control loop to regulate the output. Every time the output voltage decreases, the error voltage V_e increases and the compensator network raises V_c. So the duty cycle rises. As a result of negative feedback, the output voltage is pulled to the level of reference voltage V_{ref}. The compensation network should have several forms in dependence on required crossover frequency and parameters of LC filter **[9,10]**.

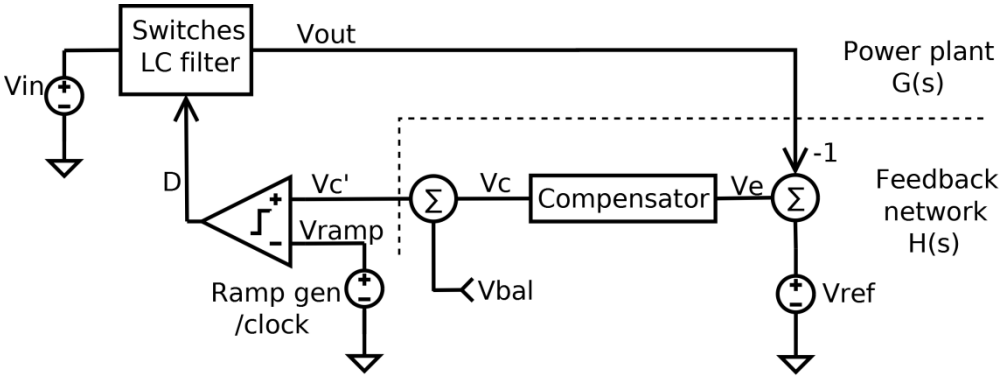


Figure 4.2.11: Block diagram of a voltage mode controlled buck **[6]**

Transfer function of power plant *G(s)* consists of:

$$G(s) = TF\_V(s) \cdot PWM_{gain} = \frac{\left(\frac{s}{\omega_{ESR}}+1\right)}{\left(\frac{s}{\omega_p}\right)^2+\frac{1}{Q}\left(\frac{s}{\omega_p}\right)+1} \cdot \frac{V_{in}}{V_{ramp}}, \quad (11)$$

where *TF_V(s)* was extracted in chapter 3.1, PWM_{gain} is gain of PWM modulator, V_{in} is input voltage and V_{ramp} is amplitude of the ramp generator which is used to generate duty cycle.

Typical transfer functions of VM controlled buck with standardized open-loop transfer function can be seen in the next figure.

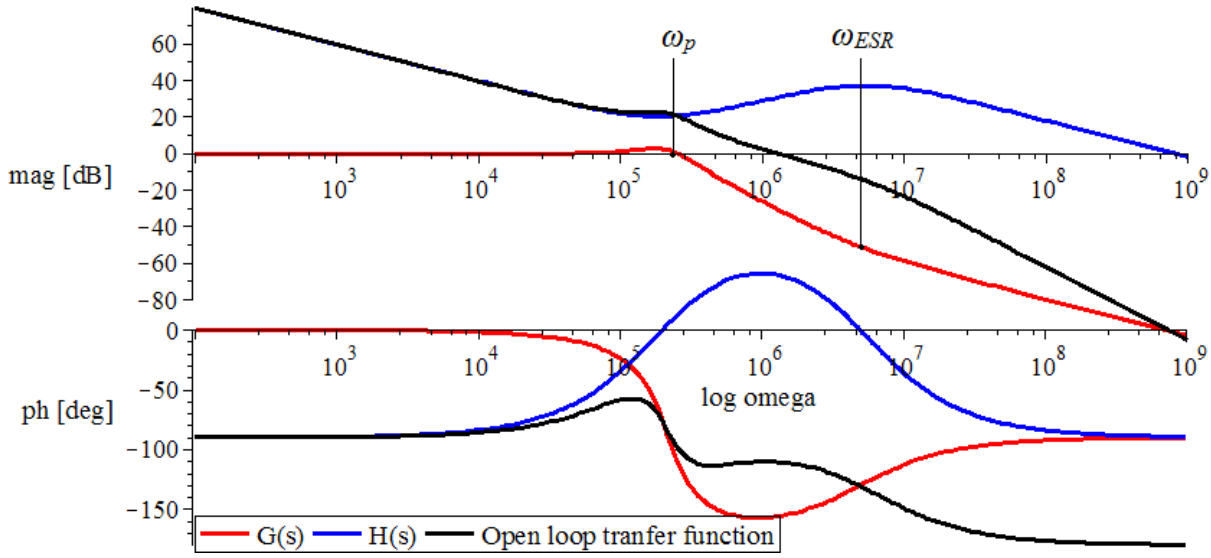


Figure 4.2.12: Typical transfer functions of VM controlled buck

This type of control suffers from line transients. When there is a change in input voltage, the duty cycle must be changed. There are two possible ways to change the duty cycle. We can simply wait for a feedback response or we can track input voltage and we can affect structure proportionally to input voltage change. This solution is known as feed-forward technique. Typically this is achieved in that the amplitude of ramp generator is proportional to V_{in}. This independence is not 100% due to imperfections, but it has additional advantage, the gain of feedback network is also independent of V_{in}.

In figure 4.2.11 there is also an example of possible input to inject balance signal V_{bal}. Because voltage mode control needs an additional current sharing loop to balance current between phases. Besides the already mentioned reasons for the current imbalance, there is another problem with the PWM generator, the comparator input offset voltage can be up in units of millivolts, it affects duty cycle. This effect limits the accuracy of the current balancing, because for all phases we have common control voltage V_c, so the control loop couldn't fix the offset. It can be improved by increasing V_{ramp}.

4.2.2 Peak current mode control

Generally, current mode control uses two feedback loops:

- faster current loop
- slower voltage loop

The faster inner current loop feeds back the information about current into the control loop as can be seen in the principal block scheme of peak current mode, figure 4.2.21.

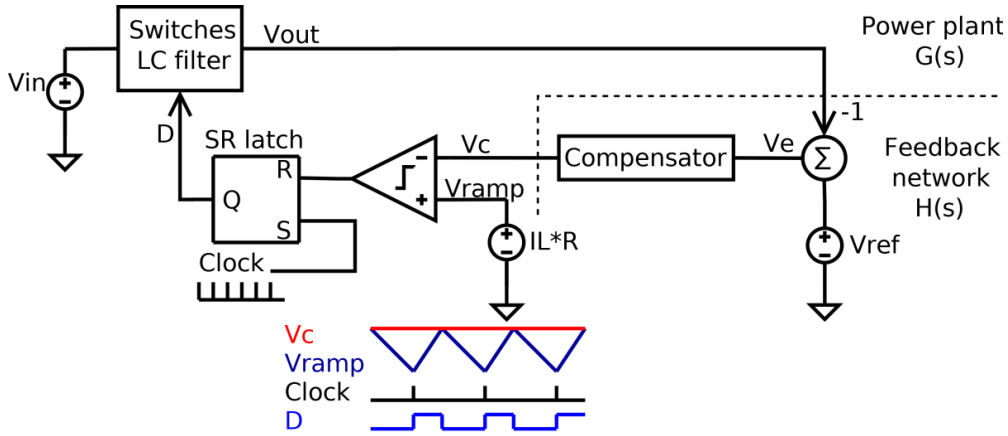


Figure 4.2.21: Block diagram of a peak current mode controlled buck **[5]**

The feedback part of this inner loop is represented by *R(s)* which is the sampling gain of the current sensor, this is usually described by Ridley's model **[11]**.

$$R(s) = R_{sen} \cdot \left(1 + \frac{s}{\omega_s \cdot Q} + \frac{s^2}{\omega_s^2}\right), \qquad (12)$$

where R_{sen} is current to voltage transfer ratio, it could be a sensing resistor, ω_s is the switching frequency and $Q = -2\pi$.

The slower outer voltage loop controls output voltage, it is similar to the control loop of voltage mode-controlled bucks, but here it controls a voltage controlled current source due to effect of inner loop. The transfer function of power plant *G(s)* has lower order than transfer function of voltage mode.

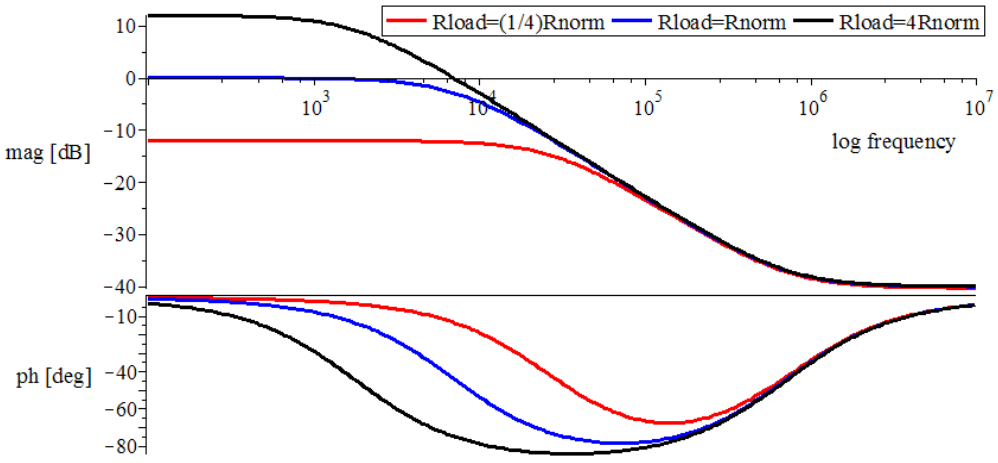


Figure 4.2.22: Typical power plant transfer functions *G(s)* of CM controlled buck for different loads

Here, the double pole characteristic is cancelled and replaced with single pole, so it is easier to design the compensator, it is because the inductor pole is located inside the current loop. But the position of pole varies with load, so the DC gain falls with high loads. The whole structure can be modelled as shown:

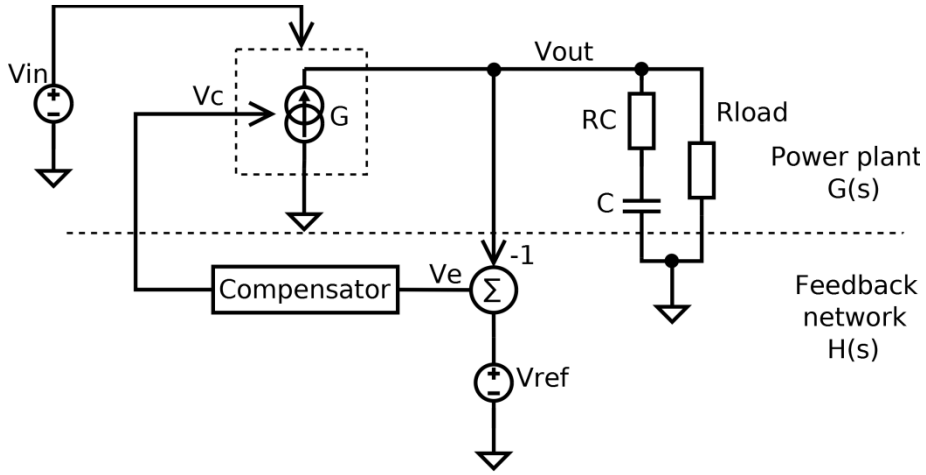


Figure 4.2.23: Simplified model of a current mode controlled buck **[7]**

Unlike the voltage mode controlled, the current mode controlled SMPSs usually have the ability to suppress line transients, because the inductor current doesn't change quickly, it is adjusted by the outer loop. This is known as pseudo line feed-forward, so the supply has good line transient performance.

A major disadvantage is the need for precise current sensing. If we use small sensing serial resistor, the current information is usually a small signal at a level of tens of millivolts. It's because we don't want to affect the efficiency. There are also other ways how to determine inductor current, but all are sensitive to switching noise. Current sensing methods are:

- voltage drop on sensing resistor
- voltage drop on MOSFET
- RC network across inductor
- current mirror/copy MOS technique

Nowadays, the last one is frequently used technique, because it is almost lossless and with enough precision. When multi-phase bucks are designed, with current mode control, it is very easy to share current among phases, which is important for high current applications. Moreover,

current sensing is integrated in most of SMPSs, because some overload protection is needed. In general, a current mode controlled converter is more reliable than a voltage mode controlled converter.

In peak current mode controlled buck the peak inductor current is controlled as can be seen from figure 4.2.21, the SR latch is reset when the inductor current rises to controlled value. But we need to control the average current for proper current balancing. There could be a current imbalance between phases due to tolerances of inductor value. Current through phase with lower inductance rises faster than through phase with higher inductance, so the average current is lower and current imbalance is appeared. The worst case occurs at light loads, as can be seen in figure 4.2.24. The output current is almost zero but the average inductor currents aren't zero. So the peak to average error is quite large, the voltage loop must correct this, which hurts response time.

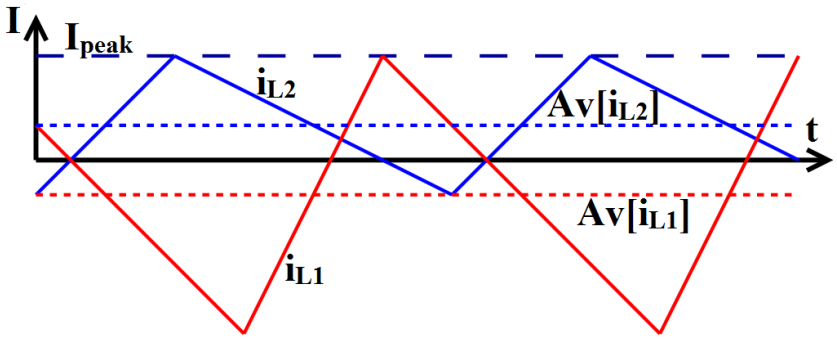


Figure 4.2.24: Two-phase CM controlled buck, $L_2 = L_1$

Typically, it is proposed that the ripple current is much smaller than the nominal current consumed by the load. It is proposed that the ripple current is much smaller than the nominal current consumed by the load. In our proposal, we expect about 3 amps per phase and the ripple current is about 10 percent, so the maximal imbalance in high load depends on the difference of inductor values, see next equation.

$$I_{ratio} = \frac{I_{out1}}{I_{out2}} = \frac{L_1 - L_2}{L_{Av}} \cdot p, \qquad (13)$$

where p is the current ripple which is defined in (4), L_{Av} is the average value of inductance.

The term sub-harmonic instability is linked to current mode control **[5,11]**. It is the major drawback. It occurs if the waveforms V_c and V_{ramp} applied to the inputs of the PWM comparator don't cross over each other at their points of intersection. This instability looks like a tendency to

oscillate at half the switching frequency and it is a duty cycle asymmetry between consecutive pulses, because the current oscillates back and forth on subsequent switching cycles. This phenomena is like any oscillation, for duty cycle $D > 50$ % is un-damped. It could be damped by an external corrective ramp, which is known as slope compensation, the oscillations decrease and die out. But the greater the corrective ramp is, the more the buck in current mode degrades its behavior to voltage mode, because the current loop gain decreases **[12]**.

4.2.3 Average current mode control

Compared to peak current mode, which compares the actual inductor current waveform to the current program level V_c at the two inputs of the PWM comparator, average current mode could have high gain current control loop, as shown in figure 4.2.31. The inner loop contains an error amplifier which is represented by transfer function *R(s)* in the block diagram, the output voltage V_i represents the average inductor current, it is compared with voltage V_c which sets the desired inductor current. The resulting voltage is compared with a sawtooth voltage of a ramp generator, its effect is determining the duty cycle.

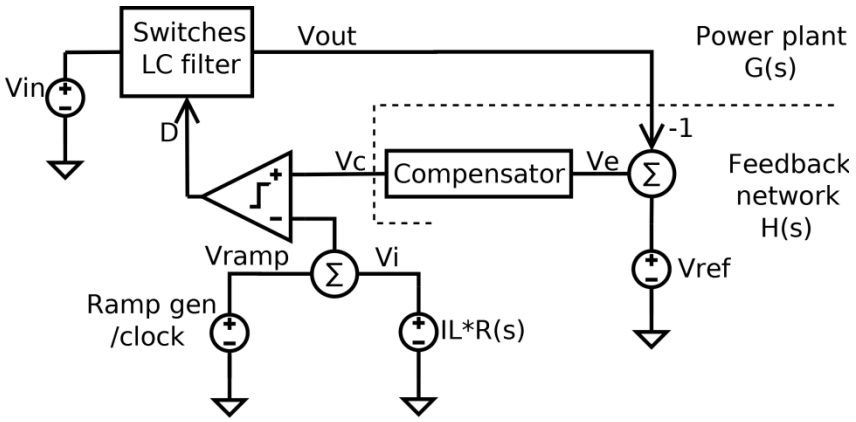


Figure 4.2.31: Block diagram of an average current mode controlled buck **[7]**

Again, this is a two loop system. The closed current loop adds a pole at the current loop crossover frequency to the voltage loop. So if the current loop crossover frequency is at a higher frequency than the voltage loop crossover frequency, than there is low loop interaction and it is easier to design voltage loop compensator.

The inner current loop gain crossover frequency could have the same value for peak and for average current mode, but the higher gain at low frequencies in peak current mode has several

advantages. There isn't a problem with discontinuous mode, because the outer voltage loop is oblivious to this mode change, in the peak current mode the gain is affected. The noise immunity is better.

Here could be also a problem with sub-harmonic instability, but in this case the slope compensation is not required due to the implemented ramp generator that provides a sufficient amount of slope compensation. There is an upper limit to loop gain at the switching frequency in order to achieve stability. The amplified inductor current slope must not exceed the ramp slope at the input of the PWM comparator.

This control mode is also suitable for multiphase buck, it has better current balancing than the previous, it holds current in phases close to each other, see the figure 4.2.24, the average current is controlled. But each phase needs a precise amplifier with defined compensation network, which enlarges the design.

4.2.4 Other current mode controls

Of course there are also other current control options. Constant on-time valley current mode control, LTC3833 is a more sophisticated example - **[6]**. This control mode architecture allows the on pulses to temporarily compress, because it doesn't need to wait for a next clock cycle in case the output voltage falls. It has shorter latency to respond to load step-up transients. This conception hasn't constant switching frequency, it isn't controlled by internal clocks and this is the most important feature for synchronizing more phases.

4.2.5 Hysteretic mode control

Hysteretic mode control is the simplest way how to control the output voltage, figure 4.2.51. Usually it is called energy on demand, it's because the output voltage V_{out} is compared in hysteretic comparator with the voltage reference V_{ref}. The output voltage ripple is proportionally set by the hysteresis window V_{win}, so when the output voltage falls to $V_{ref} - ½ V_{win}$, the HMOS switch is turned on. When the output voltage rises to $V_{ref} + ½ V_{win}$, the HMOS switch is turned off. Hence the transient response is excellent. The mathematical model is still very complicated, but it is known that the bandwidth of the loop response is close to the switching frequency. There is no feedback or compensator to design. One of the biggest advantages is that because there is no clock

and no error amplifier, the quiescent current is very low. This makes the hysteretic mode controlled buck really suitable for efficient battery powered applications.

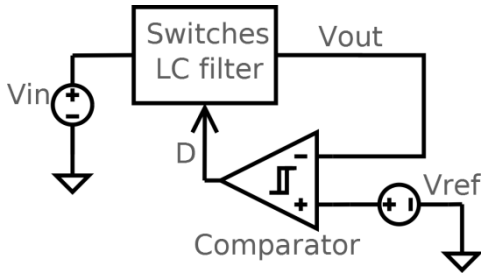


Figure 4.2.51: Block diagram of a hysteretic mode controlled buck **[8]**

As already mentioned, there isn't a clock generator, so it is impossible to assure constant switching frequency. This makes a lot of erratic pulsing, audio noise, unpredictable EMI and inability to multi-phasing. Usually adding a small replica of an inductor current ripple to one input of comparator is used to suppress multiple switching, it also helps to smooth the output voltage.

To maintain a constant frequency, there are several ways. We could automatically set the hysteresis window in accordance to the input voltage V_{in}. An involved predictor is needed, because the hysteresis window dependence couldn't be linear, unfortunately.

The next way is to use constant on-time controller. Now the hysteretic buck conception is modified, see figure 4.2.52.

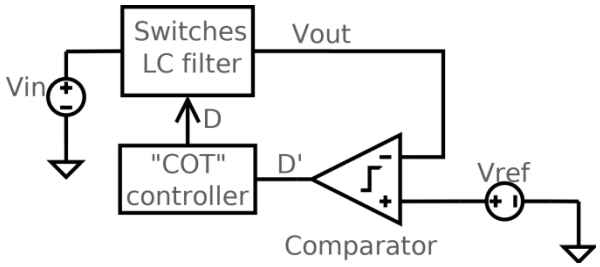


Figure 4.2.52: Block diagram of a hysteretic mode controlled buck with "COT" controller **[21]**

The hysteresis comparator is replaced by a common comparator. If the output voltage falls under the adjusted value, than the constant on-time controller generates a pulse with defined width which would be inversely proportional to V_{in}. Then the switching frequency f is nearly constant as a result of equations (14).

$$D = \frac{V_{out}}{V_{in}} = T_{ON} \cdot f, \qquad (14a)$$

$$f = \frac{V_{out}}{V_{in} \cdot T_{ON}}, \tag{14b}$$

Of course, the frequency can't be constant during load transients. Nevertheless there is no problem to create multiphase buck. In many papers the procedures are described how to achieve it. These methods are:

- interleaving - switching alternately **[13]**
- add synchronizing ramp signal **[14]**

The first method uses only one hysteresis comparator, which is the same as is used in one-phase model. The difference is in distribution of control impulses, this is shown in figure 4.2.53. For example, each odd pulse goes into the first phase and each even pulse goes to the second phase, there is no current balancing, but you can make the interleaver more smart, it could switch the phase which carry less current **[13]**. Maximal current imbalance is set by maximal inductor current ripple. Then the buck could be ringing, because phases aren't balanced linearly but in steps.

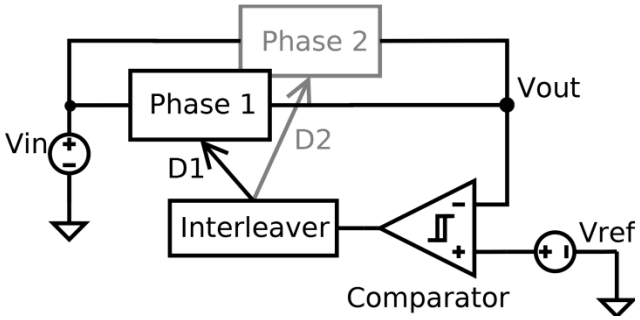


Figure 4.2.53: Block diagram of an interleaved hysteretic mode controlled multiphase buck

You can't use any amount of phases, there is a limitation of number of phases for every duty cycle. The maximum number of phases can be expressed as:

$$N_{max} < \frac{1}{D}, \tag{15}$$

where D is the expected duty cycle in which the losses correction is included (5), N_{max} is the maximal number of phases. This means that the maximum duty cycle is limited, this makes a problem when the load change occurs. The last switched-on phase is temporarily overloaded and

can result in its destruction. This disadvantage can be easily be solved by adding another comparator, which turns on all phases.

The second method is more complicated and it needs a larger change in the scheme, see figure 4.2.54. Each phase has its own hysteresis comparator to which one input a synchronising ramp is added. The ramp signal is uniformly shifted to ensure interleaving of phases. This topology isn't limited by the duty cycle as the first approach.

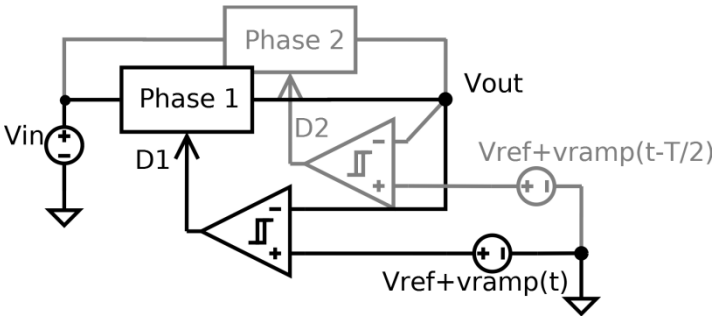


Figure 4.2.54: Block diagram of a hysteretic mode controlled multiphase buck with synchronising ramp

The added ramp emulates the output voltage ripple and its size would be around the expected hysteresis window, which defines the output voltage ripple. It is very important because the hysteretic mode controlled converter needs the output ripple to its proper function. Sometimes to smooth the output, a small replica of the phase's current ripple is also added to input of the comparator **[14]**.

4.2.6 My proposed hysteretic mode controlled multiphase buck

My intention was to design the simplest low power consumption method. My proposal is in figure 4.2.61, it is only control management without power stages, there is a draft of the most important waveforms.

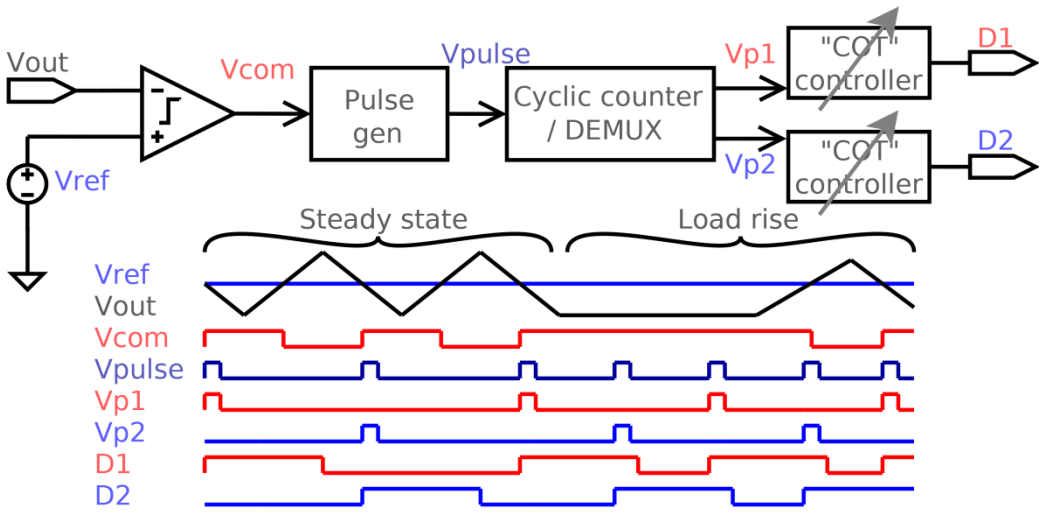


Figure 4.2.61: Block diagram of my proposed hysteretic mode controlled multiphase buck

Firstly, the output voltage is compared to the voltage reference as in all other methods, but the output voltage V_{com} goes to the pulse generator. The generator produces short pulse when a rising edge comes to its input, when the input stays in on-state for longer time than T_{pulse} next short pulse is generated. This time constant limits maximal working frequency. The generated pulses are circularly allocated to phases. In each phase, these pulses are extended to T_{ON} by constant on-time controller. This on-time and the duty cycle define working frequency in steady-state. It is necessary to observe the relationship between time constants T_{pulse} and T_{ON} (16).

$$T_{pulse} < \frac{T_{ON}}{D_{max} \cdot N_{max}}, \tag{16}$$

where N_{max} is the maximal number of phases, D_{max} is duty cycle while the input voltage is at its minimum value. If the relationship isn't satisfied, then the output never rises to the desired value. The next condition is that the loop delay must be lower than T_{pulse}.

The figure also illustrates the possibility of current balancing mechanism, it is variable on-time. I propose adding a small deviation in dependence on current imbalance. The phase which carries less current has extended on-time. This mechanism could be better than to switch the phase with less current **[13]**, you needn't to continuously know phase's currents and also the currents should be closer balanced.

4.2.7 Comparison of control mode methods

In this chapter, the main principles of control mode and their common features are explained, see table 4.2.6. There is minimum difference between current and voltage mode control, both of them have compensation network, which defines most of their parameters and increases consumption.

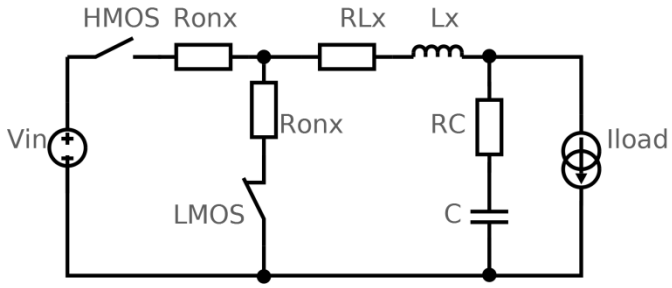
Average current and hysteretic mode control seem to be an ideal candidate for control mode of multiphase buck. The average current is good due to its easy current balance possibilities and easy multi-phasing. The hysteretic mode control has most excellent parameters. It has low quiescent current and it is easy to implement since no compensation is needed. The disadvantages are the need for current balancing loop and the problems with multi-phasing. My proposed approach with a new system for multi-phasing and current balancing could be included to this group.

	VM	Av CM	Peak CM	Hysteretic
Number of loops	1	2	2	1
Bandwidth	Depends on crossover frequency	Depends on crossover frequency	Depends on crossover frequency	Depends on comparator delay
Load transient response	Good	Good	Good	Excellent Frequency varies
Line transient response	Poor Excelent witch line feedforward	Good	Good	Excellent Frequency varies
Frequency stability	Excellent PWM ramp gen	Excellent PWM ramp gen	Excellent Pulse gen	None Poor with COT
Multiphasing	Multiphase clock	Multiphase clock	Multiphase clock	Complex Interleaving technigue for $\sum D<1$ External ramp for $\sum D>1$
Current balance	Poor	Very good	Good	Poor
Current imbalance	≈ Parasitic resistances, ΔL	Almost zero	≈((Lmax-Lmin)/Lnom)*Iripple/Iout	≈ Parasitic resistances, ΔL
How to balance	Extra loop is needed	Needless	No need	Affect Vref/ hysteretic window Affect on-time with COT

Table 4.2.6: Comparison of basic control mode methods

5. Simulation of multi-phase bucks

The simulation was performed with standard component values, see figure 5.1 a schematic of power stage. The lower index *x* indicates number of phases/power stage, in this case it goes from 1 to 4. The phases are combined in accordance to figure 2.31.



(R_{ON} = 100mΩ, R_{LX} = 50mΩ, L_X = 1uH, R_C = 10mΩ, C = 22uF)

Figure 5.1: Simulated Buck's power stage ¼

Simulated approaches are:

- VM
- Peak CM
- Av CM
- My hysteretic

For exact details and Simulink schemes of the simulated four-phase bucks, look in appendix.

5.1 Effect of tolerances to current imbalance

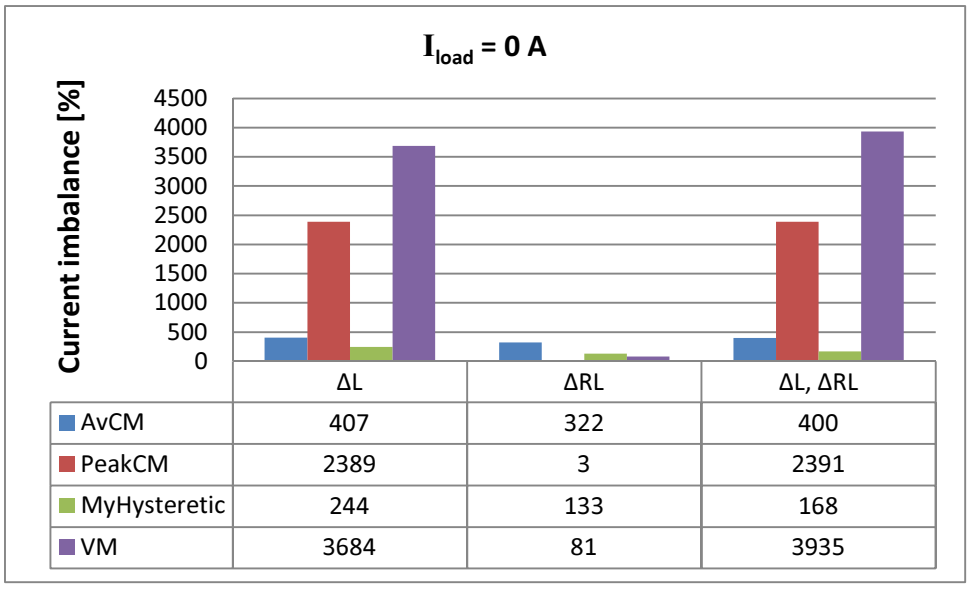
Here, the percentage of currents imbalance is verified by simulation under different output currents. V_{IN} had its typical value 3.6 V and output voltage was 1 V. Phases were modified in order to unbalance them. The list of modified parts:

- ΔL - ±50 %, L_1 = 1.5 uH, L_3 = 0.5 uH
- ΔR_L - ±50 %, R_{L1} = 75 mΩ, R_{L3} = 25 mΩ
- ΔL, ΔR_L – a variation of the previous two

In these simulations, the current balancing loops are disconnected, it relates to VM and my proposed hysteretic. Figures 5.1.1 and 5.1.2 show the simulation results, the current imbalance p_{imb} is defined in accordance to equitation (17).

$$p_{imb} = 100 \cdot \frac{MAX(ABS(I_{AV} - I_X))}{I_{AV}}, x = \{1; 2; 3; 4\}, \qquad (17)$$

where I_X is the phase current, I_{AV} is the average of phase currents. These currents represent values, which were averaged through a several switching periods in case the ripple is too significant.

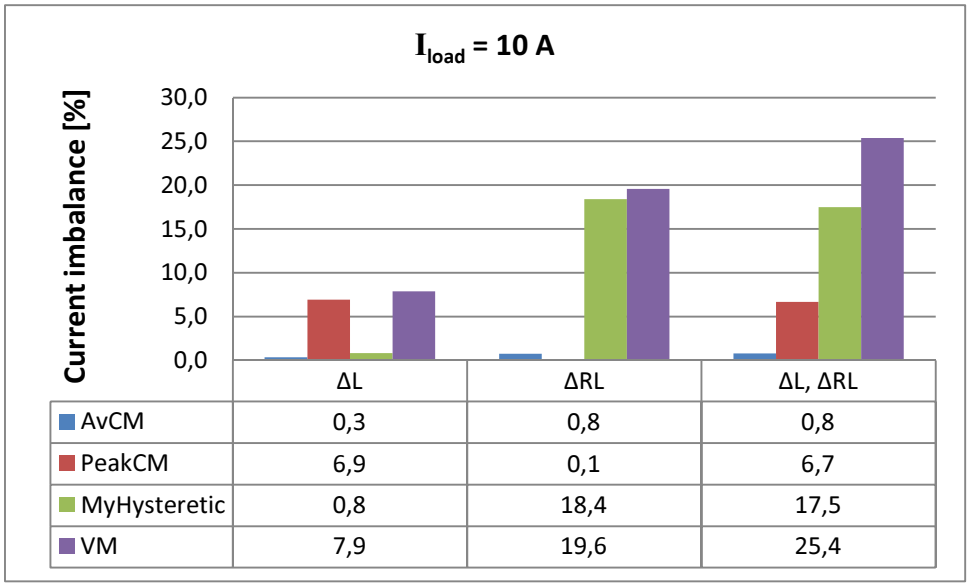


	ΔL	ΔRL	ΔL, ΔRL
AvCM	407	322	400
PeakCM	2389	3	2391
MyHysteretic	244	133	168
VM	3684	81	3935

Figure 5.1.1: Simulated current imbalance with I_{load} = 0A

At light load it can be seen what causes the current imbalance, the deviation in inductor values has major effect. But it isn't significant, for example with peak current mode control with ΔL, the maximal deviation in currents was 145 mA, which rose only to 168 mA at high load. It appears that my proposed hysteretic mode has some proper balancing ability, it has no internal current loop as a voltage mode control also hasn't, but voltage mode control has high sensitivity to inductor differences.

At high load the current mode controls have the current imbalance less than 7 % which is sufficient for most applications. My proposed hysteretic mode performs better than the voltage mode, but the current imbalance is still alarming, so a current balancing mechanism needs to be added. There is no need for such a high gain of balance amp as with voltage mode, which is important in high efficiency electronics.



	ΔL	ΔRL	ΔL, ΔRL
AvCM	0,3	0,8	0,8
PeakCM	6,9	0,1	6,7
MyHysteretic	0,8	18,4	17,5
VM	7,9	19,6	25,4

Figure 5.1.2: Simulated current imbalance with I_{load} = 10A

ΔL, ΔRL	Balancing loop	Imbalance [%]
VM	OFF	25,4
	ON	0,3
MyHysteretic	OFF	17,5
	ON	4,2

(I_{load} = 10 A)

Figure 5.1.3: Comparison of current imbalance with and without the current balancing loop

There is a verification of function of the current balancing loop which is indicated in the simulated Simulink schemes in figure 5.1.3.

5.2 Current imbalance comparison in VM and my hysteretic controlled 4-phase buck SMPS

Figure 5.2.1 shows the comparison of mode control methods without current loop, where the output current changes slowly from 0 to 10 A, this makes the measurement error due to averaging while the load is changing. The corner values can be compared with previous results, the third variant with ΔL, ΔR_L, but here the progress of current imbalance is obvious. The dependence on output capacitor is minimal, the phases are better balanced with higher value.

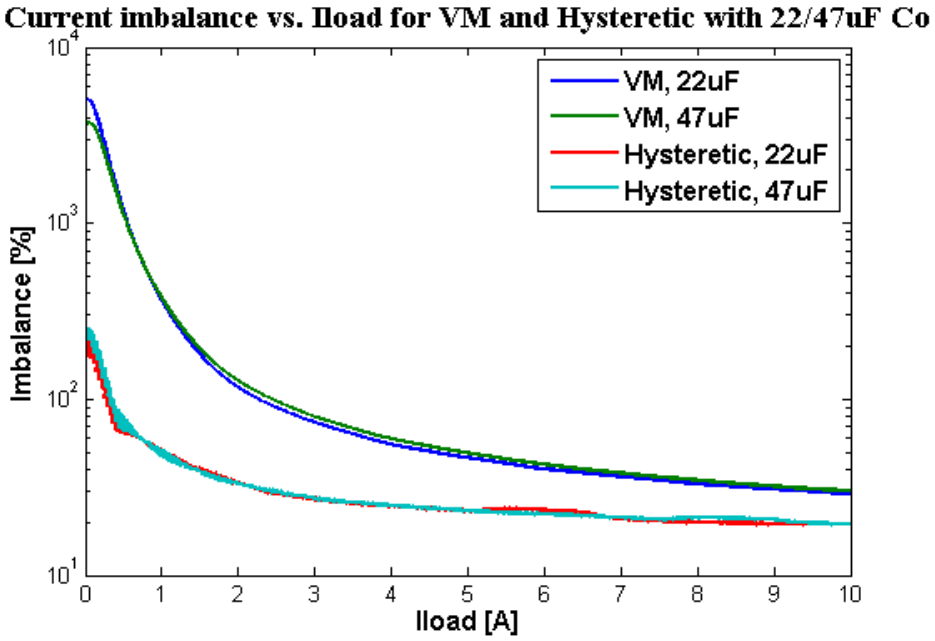


Figure 5.2.1: The current imbalance simulated in dependence on output load for my proposed hysteretic and voltage mode control

As was said, my proposed hysteretic control mode has ability to ignore difference in inductances, that is confirmed in the next simulation, see figure 5.2.2. The inductor values aren't the same. The output current is 10 A. We can observe two things. The first is that the current imbalance doesn't depend on inductances with my proposed hysteretic mode control. The second is that the phase current divergence isn't strictly proportional to phase inductance in VM. The phase sequence is also crucial, this is seen in fourth phase, which has maximal inductance, but the phase current is above average. This is caused by the voltage loop, which temporarily rises the error voltage.

	Phase	1	2	3	4	[-]
	L	1	2	4	8	[µH]
VM	I_{phase}	2,8	2,6	2,0	2,6	[A]
	Imbalance	12,0	3,7	-18,3	2,5	[%]
Hysteretic	I_{phase}	2,5	2,5	2,5	2,5	[A]
	Imbalance	0,2	-0,2	0,7	-0,7	[%]

Figure 5.2.2: The current imbalance in VM and my hysteretic mode controlled buck

In the next simulation, the differences in inductor serial resistances are adjusted proportionally to inductances. The current balance is much worse, but the hysteretic is still better, figure 5.2.3.

	Phase	1	2	3	4	[-]
	L	1	2	4	8	[µH]
	R_L	50	100	200	400	[mΩ]
VM	I_{phase}	4,1	3,0	1,8	1,2	[A]
	Imbalance	62,5	17,9	-27,9	-52,5	[%]
Hysteretic	I_{phase}	3,9	2,9	2,0	1,2	[A]
	Imbalance	56,7	17,6	-21,3	-52,9	[%]

Figure 5.2.3: The current imbalance in VM and my hysteretic mode controlled buck

So one more simulation which verifies the current imbalance depending on R_L is needed. In the simulation results in figure 5.2.4, only R_{L1} is modified and I_{out} is 10 A. The current imbalance seems to be acceptable with low tolerance of coil's R_L. In this case if we have coils with 10 % tolerance of R_L, then the low corner value is around 18 % under the high corner value and the current imbalance should be less than 5 %. Of course generally it depends on the total power stage's resistance $R_L + R_{sw}$. The maximal current imbalance p_{hyst} can be approximated by the relation:

$$p_{hyst} = 100 \cdot \frac{R_{L1}+R_{sw}}{R_{Lnom}+R_{sw}}, \tag{18}$$

where R_{Lnom} is the nominal value of coil parasitic serial resistance.

R_{L1}	50	75	90	100	150	[%]
Imbalance	14,3	6,6	2,6	0,0	-11,1	[%]
p_{hyst}	16,7	8,3	3,3	0,0	-16,7	[%]

(R_{sw} = 100 mΩ, R_{Lnom} = 50 mΩ, I_{load} = 10 A)

Figure 5.2.4: The current imbalance in hysteretic mode controlled buck

We could remove the effect of parasitic components, but an extra balancing mechanism may be needed due to non-accurately controlling the on-time by a mono-stable circuit. Every phase has one on-time controller, so they must be the same. In the figure 5.2.5 is a simulation of current imbalance in dependence on on-time variation. The on-time controllers must be matched better than 1 % due to high current imbalance.

On-time1	-3,0	-2,0	-1,0	0,0	1,0	2,0	3,0	[%]
Imbalance	-8,3	-4,9	-2,5	0,1	3,0	5,3	8,7	[%]

(I_{load} = 10 A)

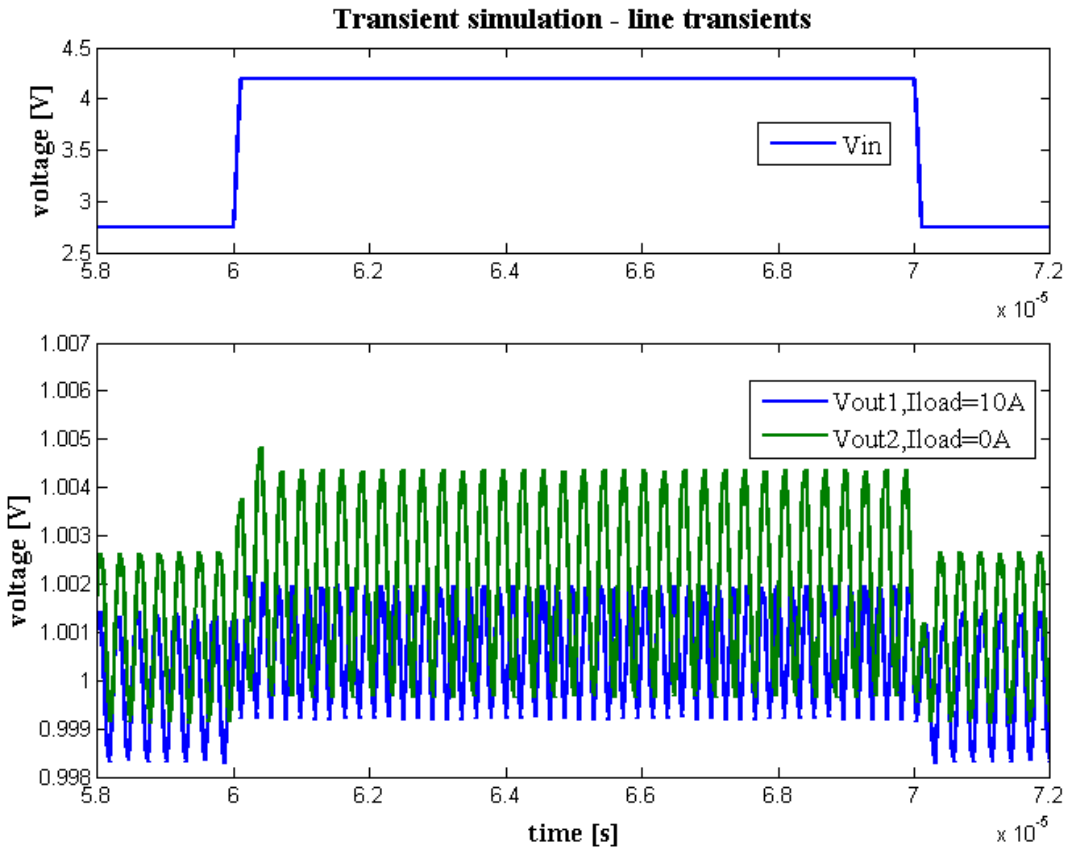
Figure 5.2.5: The current imbalance in hysteretic mode controlled buck

5.3 Testing of designed my proposed hysteretic mode controlled 4-phase buck SMPS

Finally, there are tests to determine the quality of the SMPS in terms of load. Simulations are performed with the standard values of components, unless otherwise indicated. Designed source with the proposed control method - hysteretic is tested for:

- Line transient
- Load transient

The line changes from 2.65 V to 4.2 V. The load varies between 1, 5 and 9 A. All transients have setting time 100 ns, which is less than the switching period.



(V_{ref} = 1 V)

Figure 5.3.1: The output voltage change under line transients

From the line transients simulation in figure 5.3.1, we can observe small dc offset which decreases with load rising. It's up to 2 mV with no load and maximal input voltage. It may be fixed with on-time inversely proportional to input voltage. Comparing the two waveforms, we get the internal resistance 0.10 to 0.15 mΩ, the higher value belongs to high load.

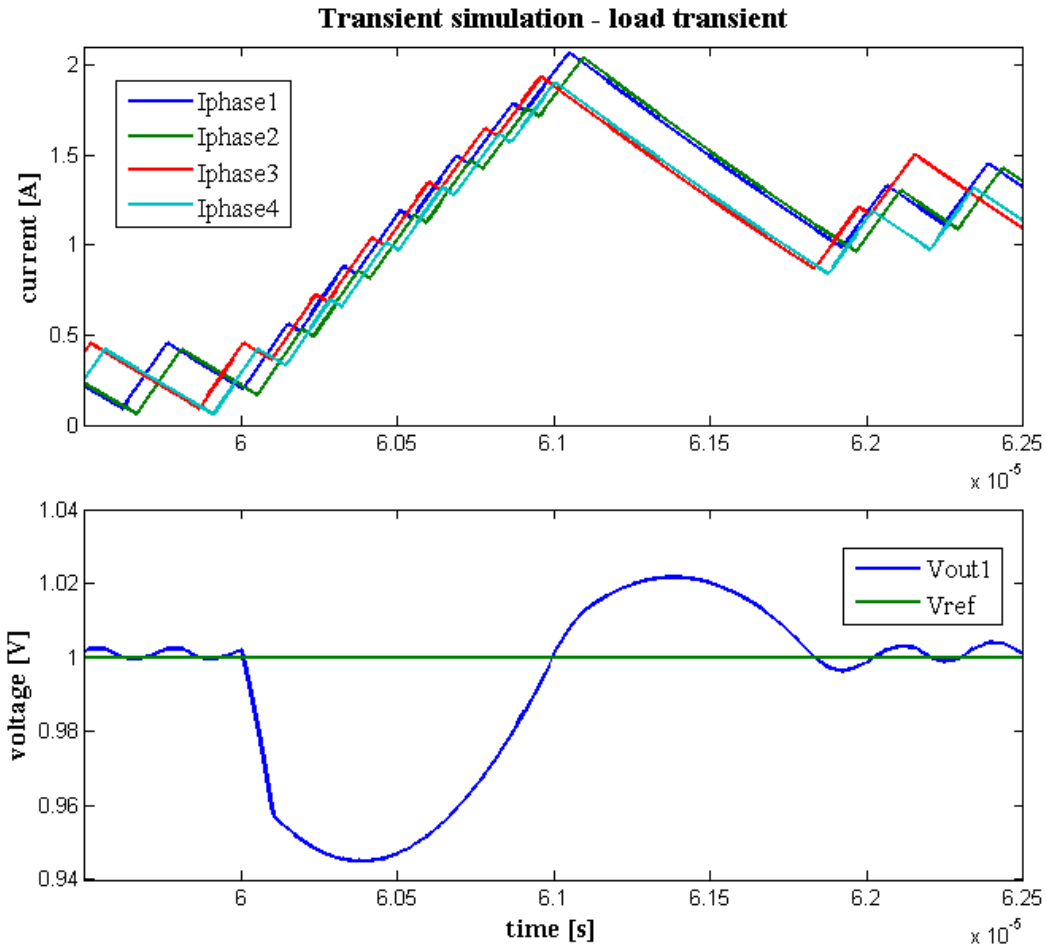
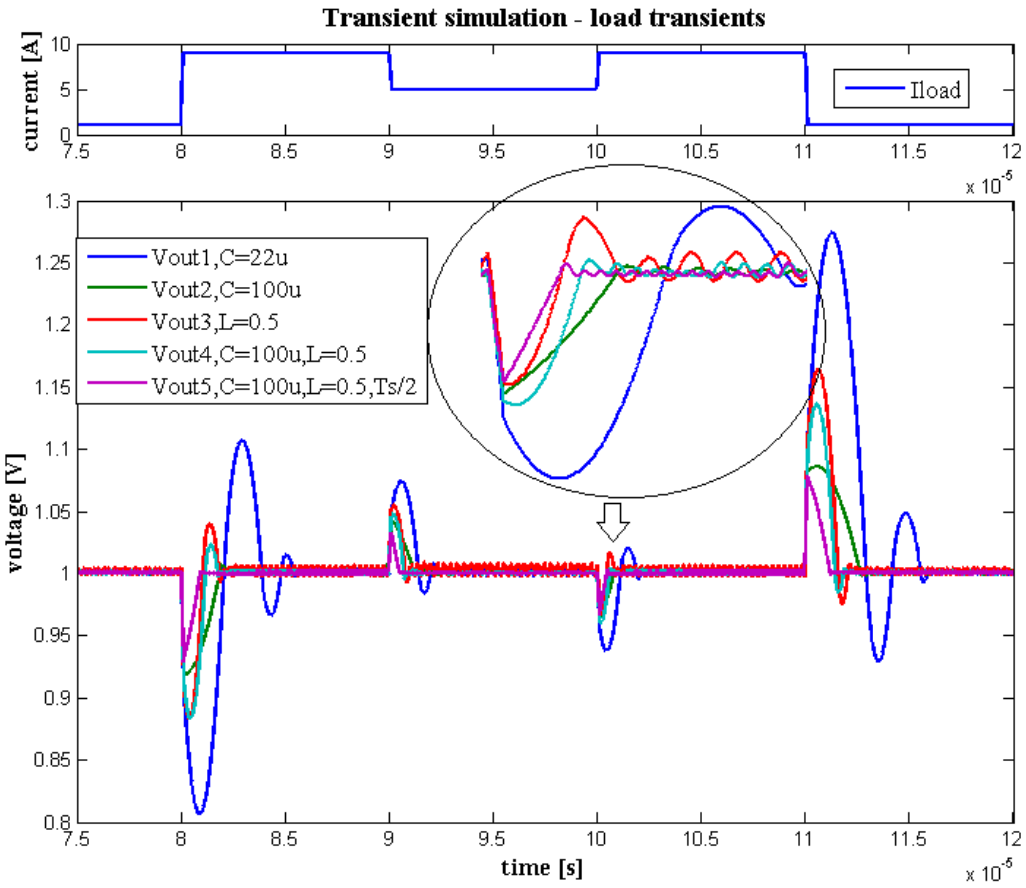


Figure 5.3.2: The output voltage change under load transient from 1 A to 5 A

In figure 5.3.2, it's a load step from 1 to 5 A. When the step comes, the undershoot appears, the main cause is effective series resistance 10 mΩ with 38 mV voltage drop. The residual drop is due to low capacitance of output capacitor, which couldn't hold the output voltage for a limited time, which is necessary to inductor current rise. This could be improved with higher capacitance of output capacitor and with lower coil inductances, see figure 5.3.3. The following overshoot is due to large amount of energy stored in coils which isn't absorbed in output capacitor. What makes it worse is that the on-time doesn't end immediately. The effective series

resistance of output capacitor also has portion on overshoot value. The output voltage tolerance with common components values is +28/-19%, with 100 µF value of output capacitor it has only +9/-8%. The tolerance range is still wide, but these large steps aren't usually expected. This depends on ARM's architecture and specifications.



(In the purple wave $T_s/2$ means that T_{pulse} and T_{ON} time constants have half values)

Figure 5.3.3: The output voltage overshoot/undershoot under load transients

This approach was chosen because of its low demand. An extra balancing loop isn't needed with proper design. It needs only one comparator for any number of phases, further signal processing could be digital. Accuracy of the time constants on chip may be around 40 %, but in this case, there is a requirement only for their precise ratios.

6. Results

The objective of this diploma thesis was:

- Design of SMPS models in MATLAB/Simulink.
- Consider the possibility of a multi-phase paralleling.
- Discuss methods for uniform load current spread in multi-phase SMPSs.
- Select the most appropriate method to power the 4-core ARM processor with a peak power dissipation 12 W (10 A @ 1.2 V).
- Evaluate the possibility of integration of chosen architecture to mobile applications.

We managed to:

- Determine the need for a multi-phase source.
- Discuss the pros and cons of multi-phase SMPSs.
- Build models of SMPSs in MATLAB/Simulink with most often used control methods.
- Define the possibility of paralleling for every mentioned control method.
- Identify key elements affecting the current imbalance.
- Design a new control method with increased inner resistance to phase asymmetry, in terms of current imbalance.
- Simulate the basic technical parameters of the proposed source.

We didn’t manage to:

- Accurately simulate the feedback networks, because they were replaced by common Simulink models, which aren’t exact models of the real components.
- Implement and verify proposal on transistor level, MATLAB doesn’t support it.

What can be improved:

- Include a battery model and input filter capacitor to model.
- Replace the feedback network models with their real models.
- Implement a solution on the transistor level, which could improve verification of other important parameters of the source.

7. Conclusion

The main goal of this diploma thesis was to design an SMPS type Buck able to supply a high consumption ARM processor. There was need to find the best solution for precise maintain needed output voltage under fast load transients. It has done with using common values of components, in case the space and technology limits exist. Next, the regulator was supposed to have high efficiency and low quiescent power consumption.

The beginning of this thesis, focuses on the basic source parameters and processor requirements. Then principles and limitations of one-phase Buck are explained. Here is also explained why a multi-phase SMPS is needed and also its pros and cons. The later used mathematical description is explained. Thereafter, the control method are investigated. This is a crucial part of the diploma thesis because the control mode defines how the output voltage is hold. And it determines the multi-phase options. In this part, I propose a new control method for multi-phase hysteretic mode control, which isn't easy to parallelize under the expected condition.

At the end, there are simulations of suitable and mostly used control methods. The most suitable method has the highest ability against non-uniform current spread between phases due to imperfections. It also needs to satisfy the conditions. Achieved results are summarized.

The whole work has done in MATLAB/Simulink not on the transistor level, so this could be the future work.

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9. Appendix

9.1 List of power stage components

C_{out} = 22 µF

$L_{1,2,3,4}$ = 1 µH

R_C = 10 mΩ

$R_{L1,2,3,4}$ = 50 mΩ

$R_{ONP,ONN}$ = 10 mΩ

R_{Load} = 50 Ω (used only in simulation for defining the power stage transfer function)

f_s = 2 MHz

f_c = 200 kHz

T_{ON} = 1.4e^{-7} s (=> f_s = 1.98 MHz in steady-state with V_{in} = 3.6 V and V_{out} = 1 V)

T_{pulse} = 40e^{-9} s

9.2 Transfer functions of power stage, PI and PID compensators

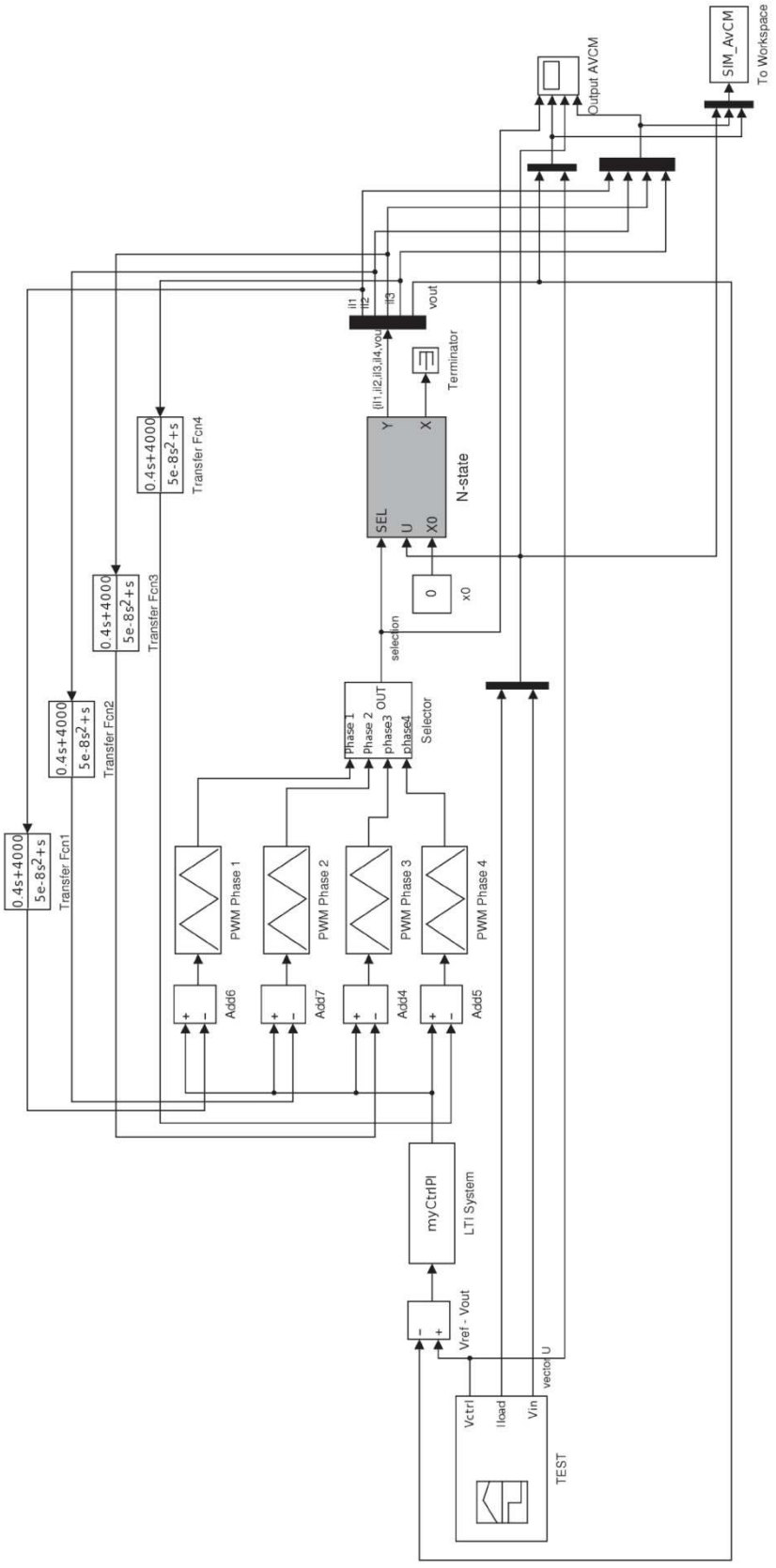
$$TF_{power\ stage} = \frac{s^4 \cdot 387e2 + s^3 \cdot 193e9 + s^2 \cdot 8{,}18e16 + s \cdot 1{,}20e22 + 5{,}94e26}{s^5 + s^4 \cdot 785e3 + s^3 \cdot 416e9 + s^2 \cdot 1{,}15e17 + s \cdot 1{,}45e22 + 6{,}68e26}$$

$$TF_{PI} = \frac{s \cdot 4{,}16 + 185e4}{s^2 \cdot 1{,}59e-7 + s}$$

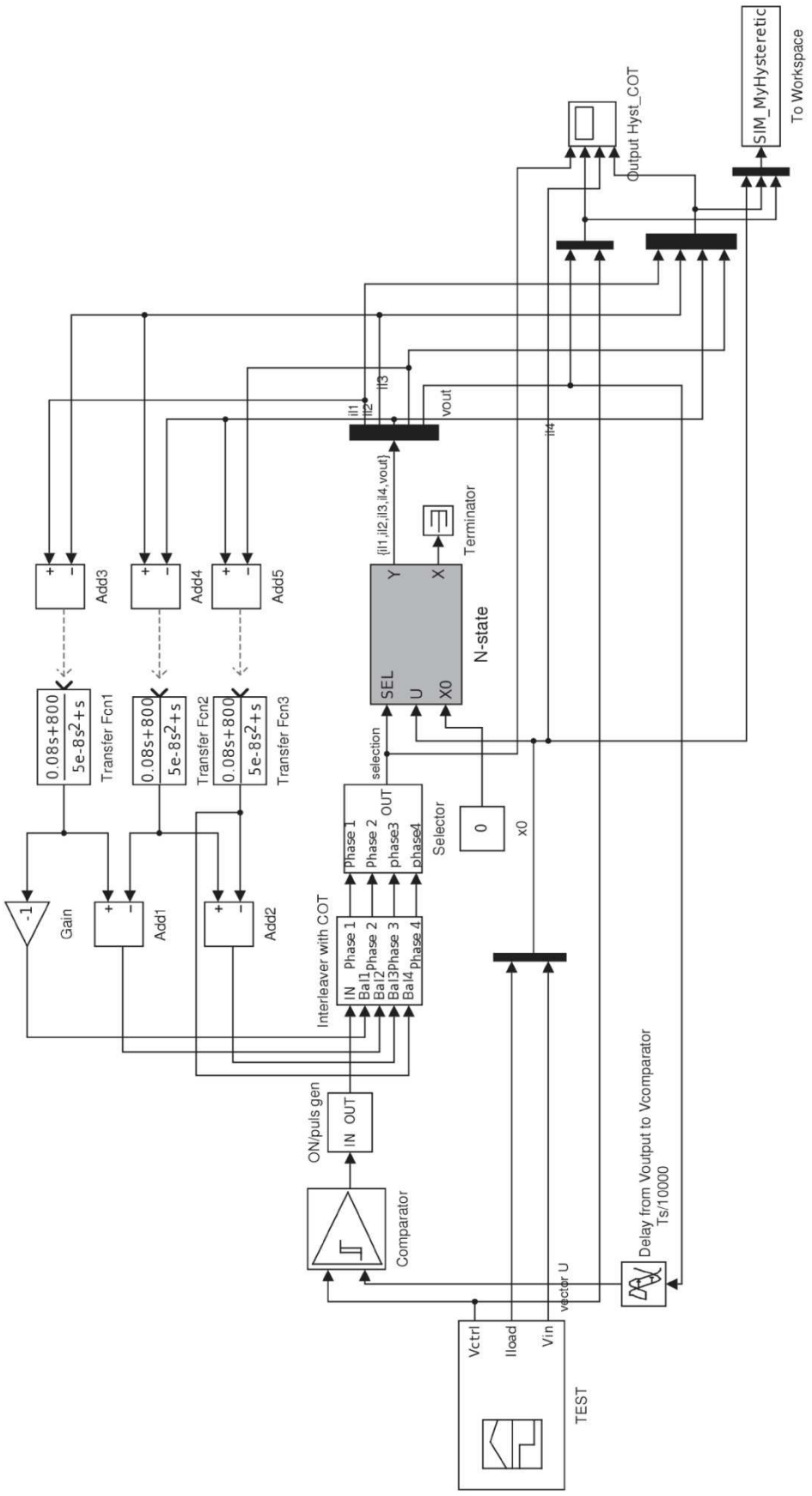
$$TF_{PID} = \frac{s^2 \cdot 6{,}07e-6 + s \cdot 4{,}72 + 901e3}{s^3 \cdot 3{,}50e-14 + s^2 \cdot 3{,}79e-7 + s}$$

9.3 Simulated schemes

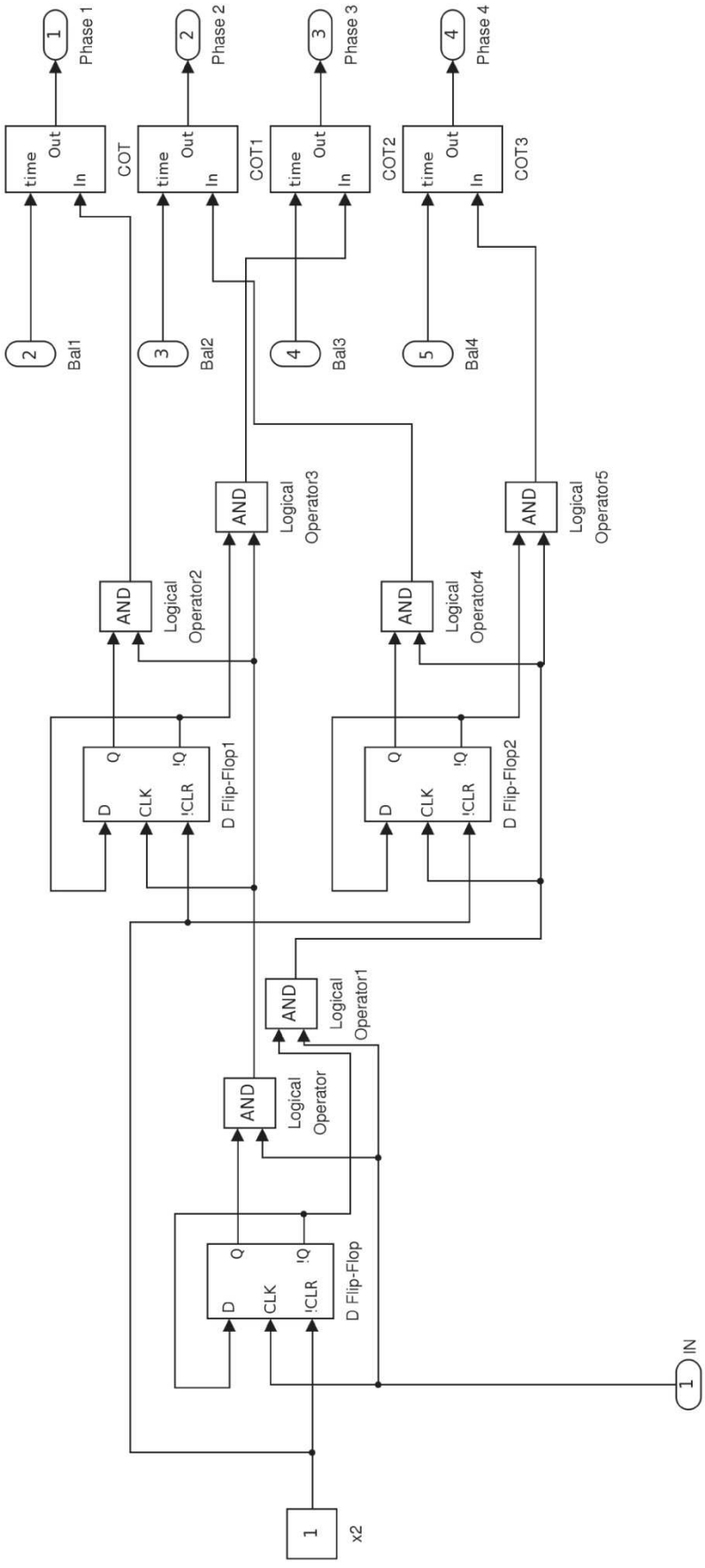
Average current mode controlled 4-phase Buck



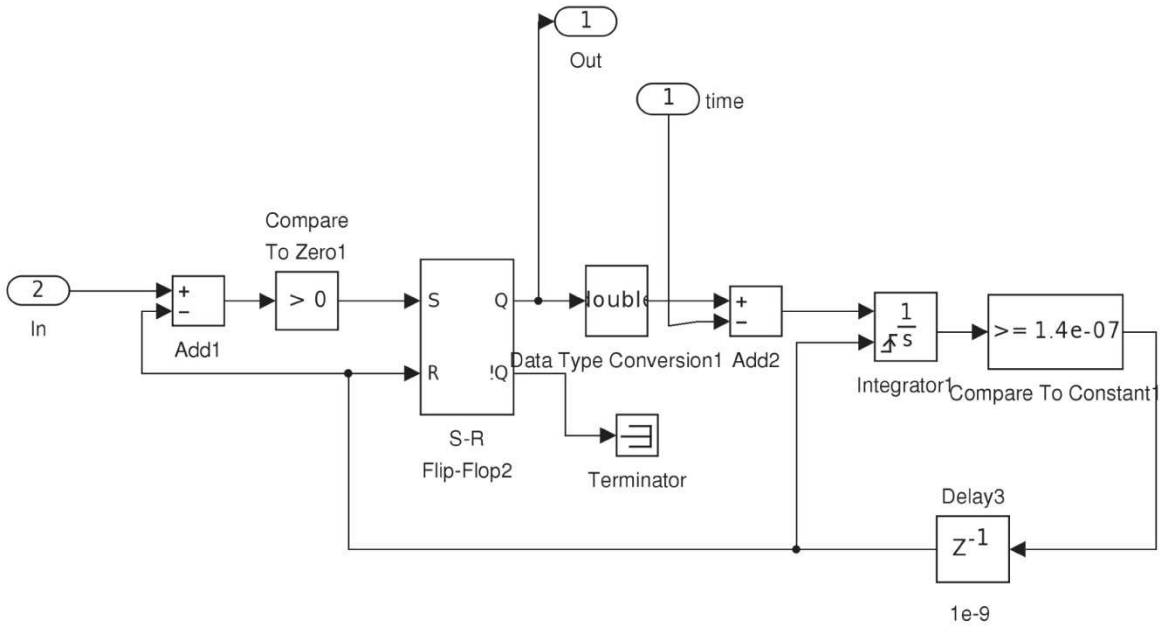
Proposed hysteretic mode controlled 4-phase Buck



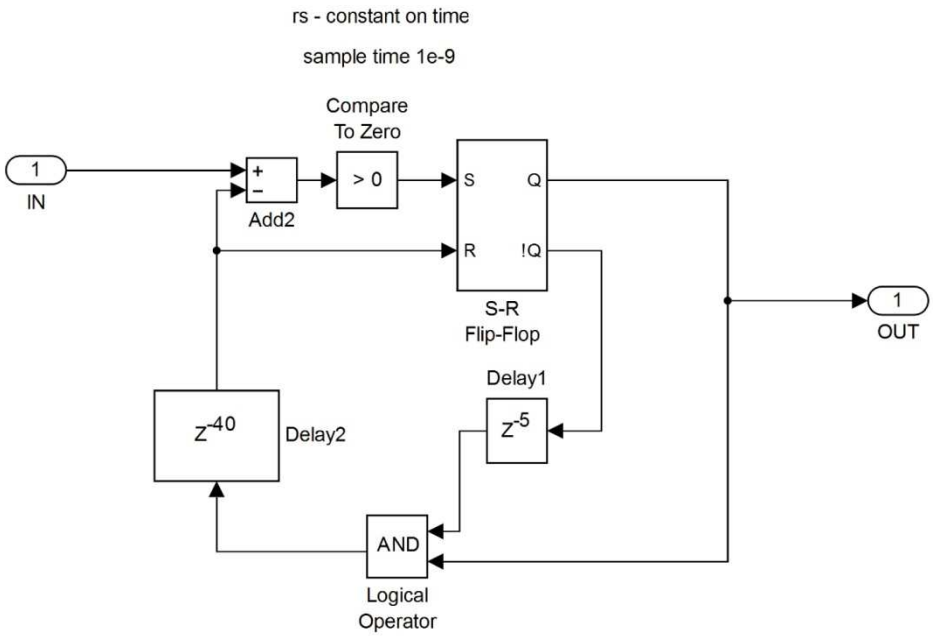
Proposed hysteretic mode controlled 4-phase Buck/Interleaver with COT



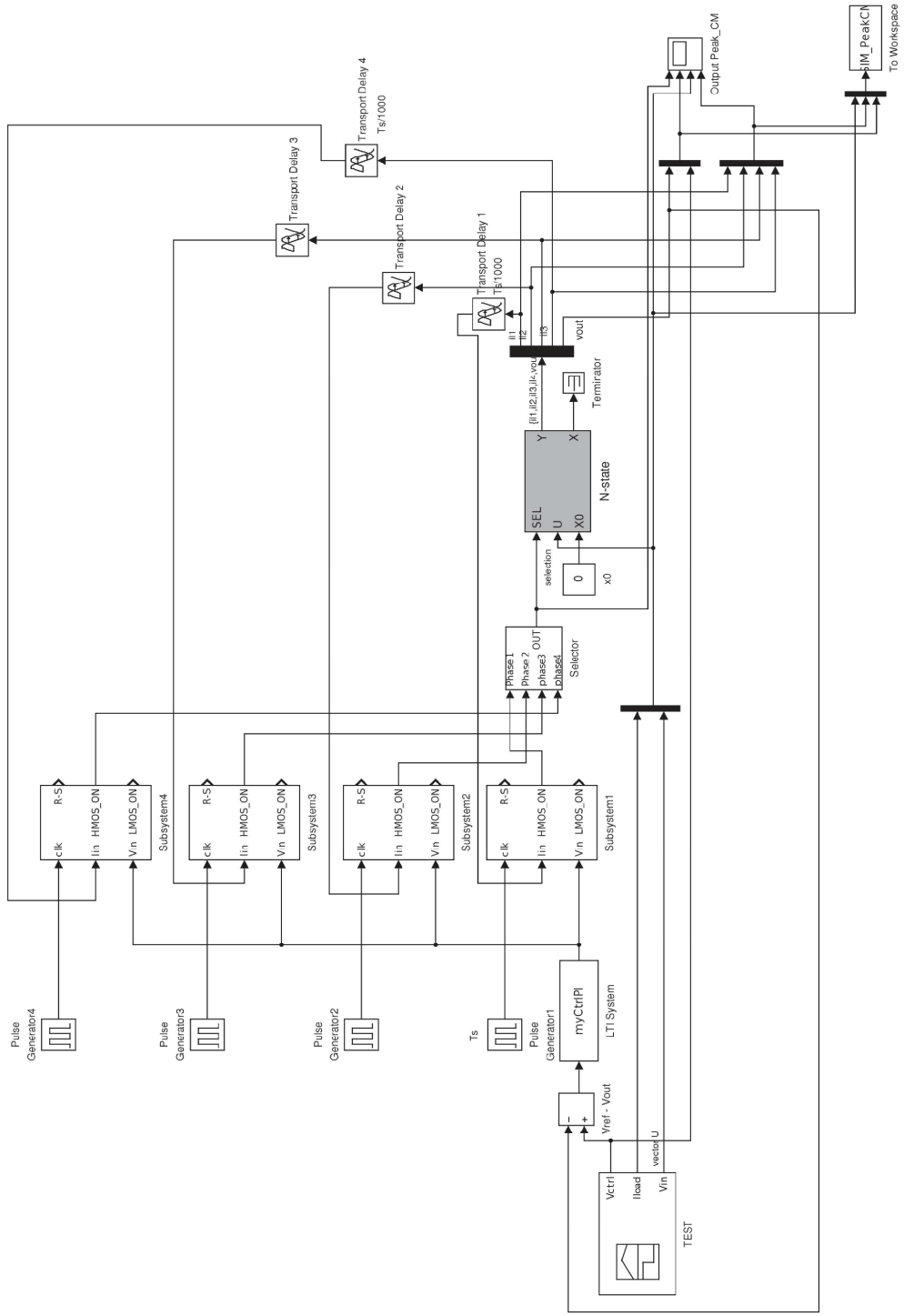
Proposed hysteretic mode controlled 4-phase Buck/Interleaver with COT/COT



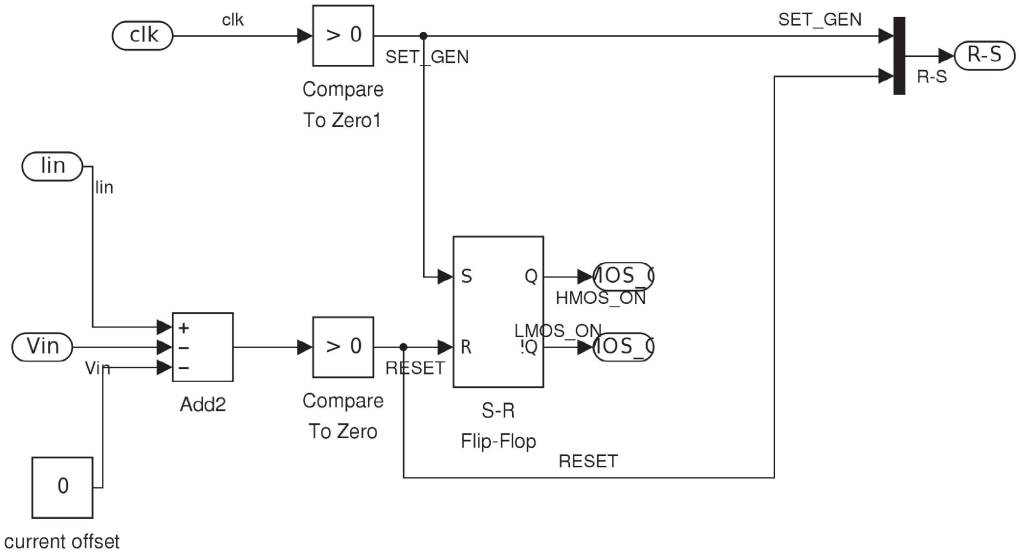
Proposed hysteretic mode controlled 4-phase Buck/ON/pulsgen



Peak current mode controlled 4-phase Buck



Peak current mode controlled 4-phase Buck/Subsystem1(controller)



Voltage mode controlled 4-phase Buck